# Circuits for a Cubic-Millimeter Energy-Autonomous Wireless Intraocular Pressure Monitor

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*Abstract*—Circuit blocks for a 1.5 $\mathrm{mm}^3$ microsystem enable continuous monitoring of intraocular pressure. Due to power and form-factor limitations, circuit blocks are designed at nanowatt power levels not completely explored before. The system includes a 75% efficient 90 nW DC-DC converter which is the most efficient reported sub-$\mu$W converter in literature. It also includes a novel 4.7 nJ/bit FSK radio that achieves 10 cm of transmission range at $10^{-6}$ BER which is also the lowest number reported for short-range through-tissue wireless links for biomedical implants. A MEMS capacitive sensor and $\Sigma\Delta$ capacitance-to-digital converter measure IOP with 0.5 mmHg accuracy. A microcontroller processes and saves IOP data and stores it in a 2.4 fW/bitcell SRAM. The microsystem harvests a maximum power of 80 nW in sunlight with a light irradiance of 100 $\mathrm{mW/cm^2}$ AM 1.5 from an integrated 0.07 $\mathrm{mm}^2$ solar cell to recharge a 1 $\mathrm{mm}^2$ 1 $\mu$Ah thin-film battery and power the load circuits. The design achieves zero-net-energy operation with 1.5 hours of sunlight or 10 hours of bright indoor lighting daily.

*Index Terms*—Biomedical monitoring, CMOS memory integrated circuits, digital signal processors, photovoltaic power systems, radio transceivers, sensor systems.

## I. INTRODUCTION AND APPLICATION DESCRIPTION

ULTRA-LOW power microsystems have become possible today due to advances in low-power integrated circuit design, improvements in fabrication technology, and the evolution of more efficient low-profile energy sources. Many biomedical applications can benefit from such microsystems. In this paper, we focus on circuits for one specific application, continuous intraocular pressure sensing for glaucoma diagnosis and management. Glaucoma is the second-leading cause of blindness, affecting over 60 million people worldwide and is predicted to impact nearly 80 million by 2020 [1]. The ophthalmological community recognizes the benefits and challenges of con-
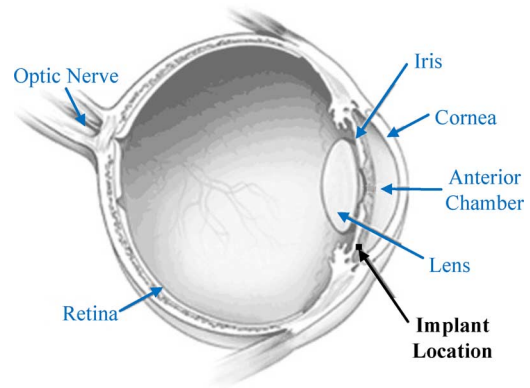
Fig. 1. The 1.5 $\mathrm{mm}^3$ IOP monitor is implanted in the anterior chamber of the eye as part of a treatment for glaucoma.

tinuous IOP monitoring, motivating previous work in this area [2]–[6]. A contact lens approach measures IOP by measuring the deformation of the cornea curvature due to IOP changes [7]. This reduces patient intervention, but requires an external power source from an eye patch surrounding the eye of the patient. Typical usage is limited to a 24 hour time period. Another recent implanted solution stores energy on a 24 $\mu$F capacitor array to continuously collect data over a 24 hour period, but requires a 27 mm antenna for data and power transfer [8].

One primary factor that distinguishes the proposed intraocular pressure sensing microsystem (IOPM) from previous work is its small 1.5 $\mathrm{mm}^3$ form factor that enables us to implant it in the anterior chamber of the eye (Fig. 1). From a circuit perspective, the major challenge is to design all the system components shown in Figs. 2 and 3 such that they do not exceed the power budget of the system. Table I shows the main circuit-level limitations on the system. In order to realize these goals we introduce novel blocks with record-low energy consumption and apply analog and digital low-power techniques to other blocks to keep average and peak power consumption below the values dictated by the small thin-film battery.

As shown in Fig. 3, the monitor contains two integrated circuit (IC) chips fabricated in a 0.18 $\mu$m CMOS process. The top IC contains a solar cell and fully-integrated wireless transceiver (TRx). The bottom IC contains a sigma-delta capacitance to digital converter ($\Sigma\Delta$ CDC), microprocessor ($\mu$P), and static random access memory (SRAM). The solar cell and a thin-film solid-state Li battery deliver power to the microsystem through the power management units (PMU), allowing microsystem operation without patient intervention for power delivery. Ambient light is used for energy harvesting, and wireless communication signals easily penetrate the package to form a bidirectional interface with the outside world. A 2 mm × 1.5 mm
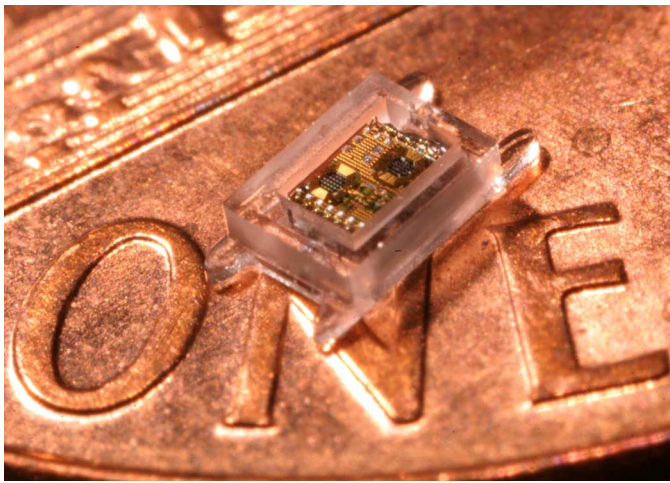
Fig. 2. IOP monitor microsystem photo and diagram. The top of the glass enclosure is omitted in the photo to highlight circuit components.

MEMS capacitive sensor forms the bottom layer as shown in Fig. 3 [9]. All these blocks are encapsulated in a sealed glass container. The biocompatibility of the glass container has been demonstrated through implantation and in-vivo measurements in the eye [10]–[12].

Section II describes a $\Sigma\Delta$ CDC that achieves $2 \times$ sensitivity improvement over previous IOP monitors [13]. Section III describes the design of an ultra-low-power 8-bit microcontroller and SRAM which achieve the lowest average power to date. Section IV explains the novel dual-resonator FSK transceiver that enables us to achieve 10 cm of through-tissue transmission at an energy consumption of 4.7 nJ/bit. Section V covers the design of the switched capacitor circuit that is, to authors' best knowledge, the most efficient sub-$\mu$W DC-DC converter to date. Finally, Section V draws the conclusion of the paper.

## II. CAPACITANCE TO DIGITAL CONVERTER

### A. Capacitance to Digital Converter Background

Capacitance to digital converters (CDCs) apply an excitation force to a variable sensor capacitance to generate a voltage, current, or time and then use analog to digital (ADC) techniques to output a digital value. Simple readout circuitry charges and discharges the capacitance at one node of a CMOS ring oscillator, and measures the oscillation frequency. However, this method is highly dependent on process, voltage and temperature variations. A 500 $\mu$W capacitance to digital converter design incorporates the sensor capacitance into the digital to analog converter portion of a successive approximation register (SAR) ADC [14]. SAR ADCs have been demonstrated with figures of merit as low as 4.4 fJ/conversion step in a 1.9 $\mu$W design [15]. Several capacitance to digital converter designs incorporate the sensor capacitance as a switched-capacitor resistor in an integrating amplifier to achieve accuracies within 19.3 aF [16]–[18]. The slope of the integrator output is proportional to the pressure sensor capacitance. The integrator output ramp can be digitized using $\Sigma\Delta$ or pulse-position modulation (PPM) ADCs, with a demonstrated 5.6 $\mu$W $\Sigma\Delta$ ADC achieving 303 fJ/conversion step [19] and a 14 $\mu$W PPM ADC achieving 98 fJ/conversion step [20].



Fig. 3. IOP monitor block diagram and die photos.

TABLE I
CIRCUIT CONSTRAINTS ON IOPM

| Module | Requirement | Achieved |
|---|---|---|
| CDC Sensitivity | 1mmHg | 0.5mmHg |
| CDC Active Power | 10 $\mu$W | 7 $\mu$W |
| Radio Energy/bit | 7 nJ/bit | 4.7 nJ/bit |
| Total Stand-by Power | 5nW | 3.3nW |
| Total Silicon Area Including Decap, TRx Coils, and Pads | 1.8mm$^2$ | 1.8mm$^2$ |

### B. Capacitance to Digital Converter Implementation

The capacitance to digital converter for the IOP sensor is designed to achieve low sensitivity to process variation, voltage fluctuations, and clock uncertainty with low peak and average power. Precision is improved using differential measurements with common voltage and frequency references. 7.0 $\mu$W active

Fig. 4. The capacitance to digital converter generates a pressure-sensitive current by switching the pressure sensor and measures the pressure sensor capacitance with $\Sigma\Delta$ modulation.



Fig. 5. The pressure sensor and capacitance to digital converter achieve 0.5 mmHg IOP accuracy with high linearity.

power is achieved by generating small excitation currents using weakly inverted devices and eliminating integrating amplifiers found in typical $\Sigma\Delta$ converters.

The CDC measures the capacitance of the pressure sensor ($C_{MEMS}$) by differentially comparing it to 250 fF fixed MIM capacitors ($C_1, C_2$) (Fig. 4). The capacitors are used to generate pressure-sensitive and fixed currents by using them as switched-capacitors and then applying a fixed voltage across them. These difference of the pressure sensitive and the $\Sigma\Delta$ modulated fixed current is accumulated onto an integration capacitor ($C_{INT}$). The fixed current is duty cycled to regulate the voltage on $C_{INT}$ at $V_{3P6}/2$. The voltage on $C_{INT}$ ($V_{INT}$) is compared with $V_{3P6}/2$ using a clocked comparator and device $M_{P1}$ is modulated with $\Sigma\Delta_{OUT}$ to control $V_{INT}$. $\Sigma\Delta_{OUT}$ is accumulated into a 14 b digital value with a 10,000:1 decimation filter that counts the number of cycles where $\Sigma\Delta_{OUT}$ is high over a 10,000 clock cycle period to generate the digtal measurement of sensor capacitance.

$\Sigma\Delta$ modulation cancels out quantization and temporal noise and also devices and references are carefully matched allowing higher accuracy with lower power circuits. The capacitors are switched using a shared 50 kHz clock to reduce clock sensitivity. $C_1$ and $C_2$ use 180° out of phase clocks ($\Phi_1, \Phi_2$) to create a more-constant fixed impedance, yielding better results than switching a single 500 fF MIM capacitor.. A fixed voltage is dropped across the switched-capacitor resistors to generate both a pressure-sensitive and a fixed current. This voltage drop is regulated with saturated transistors $M_{N1}$, $M_{N2}$, and $M_{N3}$. A reference voltage equal to $V_{3P6}/2$ is generated using a 2:1 switched capacitor divider and connected to the gate of the current limiting devices. Since $V_{3P6}/2$ is shared, the capacitance to digital converter output also has reduced sensitivity to $V_{3P6}$.

Low power techniques are carefully applied in the CDC to decrease overall IOP energy usage and reduce the amount of harvested energy required for energy autonomy. A 50 kHz ring-oscillator-based clock is chosen to satisfy CDC power requirement in Table I. This requirement comes from the maximum continuous current the thin-film battery can supply before its voltage drops more than 100 mV. The microsystem's battery can supply at most 40 $\mu$W, so to reduce power the capacitance to digital converter generates a 0.9 V 50 kHz clock with a current-starved ring oscillator, and then converts it to a 3.6 V clock for the switched capacitor resistors and comparator. The slow clock saves power by decreasing the pressure-sensitive and fixed currents and also reducing the activity and power of the comparator. However, since capacitance to digital converter accuracy is related to the number of clock cycles, using a slower clock does not reduce the energy per measurement. Energy per

measurement is inversely related to clock frequency because of increased leakage energy over a longer measurement time period. Static current is decreased by using an integration method that does not require an amplifier, avoiding the power overhead for its quiescent current. Between pressure measurements, the clock is disabled and only leakage power is consumed. To reduce leakage power, all transistors in the capacitance to digital converter are ultra high threshold voltage, thick-gate oxide (UVT) devices with leakage power that is three orders of magnitude lower than logic device leakage.

### C. Capacitance to Digital Converter Measurement Results

The MEMS capacitive pressure sensor is placed in a pressure chamber and connected to the capacitance to digital converter for measurement. The pressure range of interest for IOP measurements is 0–60 mmHg above atmospheric pressure, with healthy IOP ranging between 10–21 mmHg. Higher pressures can indicate glaucoma [21]. The pressure sensor has a resolution of 26 fF/mmHg [22]. Pressure sensor hysteresis effects contribute 1 mmHg of uncertainty to the pressure measurement. Goldmann applanation is the golden standard for IOP measurements and achieves 1 mmHg accuracy. The capacitance to digital converter has 0.5 mmHg accuracy, which translates to 13 fF, while consuming 7.0 $\mu$W active and 173 pW standby power (Fig. 5). The standard deviation is less than 0.5 mmHg with 50 measurements taken at each pressure. The output is highly linear due to the contact-mode pressure sensor and switched-capacitor capacitance to digital converter techniques. The differential non-linearity (DNL) is 0.31 LSB and the integrated non-linearity (INL) is 1.54 LSB, calculated using end point linear calibration which were within the range of expected results based on simulations across process corners.

Although body temperature is well controlled, the outer eye does experience some temperature fluctuations on the order of 10 °C [23]. To reduce temperature sensitivity, the capacitive sensor is sealed in vacuum to mitigate the effects of thermal expansion. The fixed MIM capacitors in the capacitance to digital converter also exhibit low temperature dependence. The temperature sensitivity of the capacitance to digital converter is 5.6 mmHg/°C as shown in Fig. 6(b). From [23], we expect the temperature at the surface of the iris to vary between 15 °C and 40 °C in extreme external environments. This error due to temperature variations would need to be calibrated out with an external temperature measurement. This measurement can be done by adding a sub-$\mu$W temperature sensing module similar to [24] to IOPM. Measurements of the pressure sensor used in this work indicate drift of less than 0.5 mmHg over the course of 2 weeks, which is most likely due to mechanical wearing of sensor membrane under pressure. Long-term in vivo sensor drift
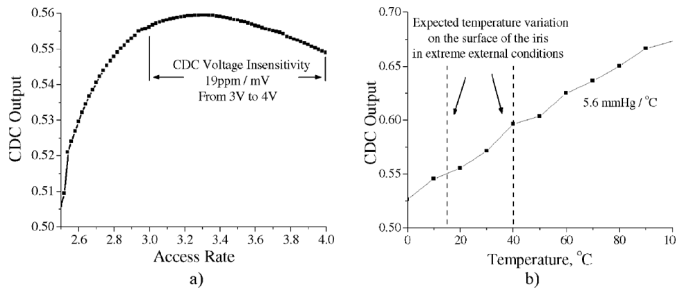
Fig. 6. Pressure measurement sensitivity to variations in a) battery voltage and b) temperature.

studies would be useful in assessing the impact of scar tissue build-up on the sensor on IOP measurements.

## III. MICROPROCESSOR AND MEMORY

### A. Microprocessor and SRAM Background

There has been significant previous work on low-power microprocessors and SRAM [25]. $V_{DD}$ scaling reduces dynamic energy quadratically and leakage power exponentially. However, delay degrades resulting in increased leakage energy per microprocessor instruction. The competing trends in dynamic and leakage energy lead to an intermediate near-threshold or sub-threshold $V_{DD}$ where total energy per instruction is minimized [25]–[28] . Numerous designs have applied $V_{DD}$ scaling to custom and commercial microprocessors to achieve energy as low as 2 pJ per instruction [29], [30]. To ensure low-$V_{DD}$ functionality, previous works remove high fan-in standard cells and perform extensive Monte Carlo analysis of sequential elements [29], [31] . When inactive, the microprocessor consumes only leakage power. Optimal technology selection balances active and standby energy for the microprocessor based on its duty cycle [32]. Power gate size should be chosen to minimize leakage while meeting performance requirements, which are often loose in ultra-low power sensor applications [31]. The power gate can be implemented as a low-leakage UVT device and then overdriven with $V_{BATT}$ to maximize on-to-off current ratio [33].

Processor data can be stored in volatile or non-volatile memories. Non-volatile memories such as embedded Flash do not require power to retain data, making them good candidates for reducing standby mode power [34]. However, these memories have high write powers, require high write voltages, and are not readily available to academic researchers. SRAM is easily designed in CMOS processes using only the nominal voltage. However, data retentive SRAM cannot be power gated without data loss, so minimizing SRAM leakage is vital for achieving energy-autonomy. $V_{DD}$ scaling in SRAM reduces energy but degrades stability margins [35]. An 8T SRAM bitcell separates read and write constraints to improve stability [36], [37] . A 10T SRAM approach further improves read stability by pulling up read bitlines (BLs) and reducing read buffer leakage [38], [39] . The IOP microsystem includes a 9.8 pW 0.45 V 4 kb ultra-low-leakage 10T SRAM. The SRAM bitcell uses UVT devices and gate length biasing in the data-retaining portion while power gating the read buffer to achieve 2.4 fW/bit standby leakage [40]. The SRAM drives the BLs at 0.9 V to improve write stability, and employs PMOS pass gates because they are

faster at the $V_{DD}$ of interest and hierarchical BLs to reduce latency.

### B. Microprocessor and SRAM Implementation

The microprocessor coordinates data transfer and management among the capacitance to digital converter, wireless transceiver, and SRAM. After a capacitance to digital converter measurement is complete, the microprocessor wakes up from standby mode and reads the result from a memory mapped location. The microprocessor can perform digital signal processing (DSP) to extract useful medical information from raw IOP data as well as perform data compression. Simple examples of DSP include detection of the average, peak, or changes in IOP over a time interval. This analysis is facilitated by the linear relationship between pressure and capacitance to digital converter output. The microprocessor can also be used to compress IOP data, reducing memory footprint. The full-range capacitance to digital converter output ranges from 0–10 000 with a 14 b digital representation. However, over the pressures of interest, the output range is 180 allowing the microprocessor to compress the data to an 8 b value. Storing differential instead of absolute IOP values further reduces memory footprint, enabling leakage reductions through power gating of unused SRAM banks during standby mode. After processing the data is stored into SRAM. When the user generates a wireless wakeup event, a separate microprocessor program is called. This program receives wakeup signals from the transceiver, retrieves data from SRAM, and initiates wireless transmissions.

Low-power techniques in the microprocessor and SRAM reduce active mode peak power and standby-mode-limited energy consumption. The microprocessor is an 8 b microcontroller with an instruction set that supports 16 registers. In the 8 b instruction, 4 bits are an instruction operand. For 15 operands, the other 4 instruction bits denote a register. These instructions compute operations between the designated register and a general purpose register that is used in every instruction. The $16^{TH}$ operand performs special tasks based such as initiating a transceiver transmission and entering standby mode. $V_{DD}$ is scaled near the minimum energy point, thus, $\mu$P and SRAM consume 90 nW at 0.45 V. In standby mode, an NMOS UVT header transistor virtually eliminates the microprocessor's contribution to standby mode power. In active mode, this header is overdriven with $V_{BATT}$ to meet the 100 kHz performance target.

## IV. WIRELESS TRANSCEIVER

### A. Transceiver Background

Wireless transceivers for medical implants are limited by antenna size and power budget constraints. Passive backscattering techniques bypass transmitter power budget limitations by reflecting an incoming RF signal using impedance modulation. These techniques achieve a $10^{-6}$ transmit bit error rate (BER) over a 2 cm transmission channel with a 3.5 cm diameter coil [41] and a $1.5 \times 10^{-6}$ BER over 15 mm with a 40 mm coil [42]. However, these devices are too large for IOP monitoring. Active techniques draw from microsensor power supplies to achieve higher transmit performance with smaller antennas or coils. These transmitters achieve energy efficiencies as low as 20.4 nJ/bit with coils as small as 0.47 mm [8], [43]–[46]. Previous transceiver implementations consume higher peak
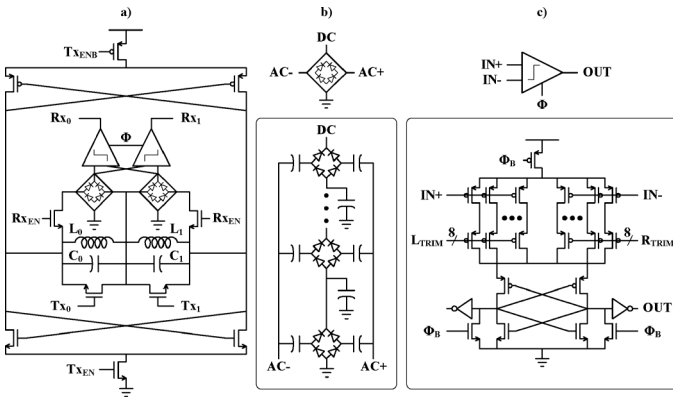
Fig. 7.  (a) The transceiver uses a dual-resonator with a combined local oscillator and power amplifier. (b) The multi-stage rectifier. (c) The variable offset comparator.

power than the 1 mm$^2$ battery can source and limit device lifetime because of high leakages.

### B. Transceiver Implementation

The fully-integrated transceiver receives wireless wakeup signals and responds with IOP data. It uses FSK modulation with two tones at 433 MHz and 915 MHz in the industrial, scientific, and medical (ISM) bands. The doctor or patient places an external wand over the eye and transmits a wireless wakeup signal to activate the IOP monitor. The receiver is activated (Rx$_{EN}$) and generates one of two digital signals (Rx$_0$, Rx$_1$) based on the wakeup signal frequency (Fig. 7). The wakeup signal is coupled onto one LC tank of the dual-resonator structure and connected to the rectifier with a switch controlled by Rx$_{EN}$. The ac signal is converted to dc using one of two 8-stage full-bridge rectifiers. The dc offset is then converted to the digital Rx$_0$ and Rx$_1$ signals by comparing the dc outputs of the rectifiers with two 50 Hz variable-offset comparators. Thus, the Rx$_0$ or Rx$_1$ is generated when more RF energy is received on either half of the dual-resonator tank than the other, indicating a wakeup signal at the intended frequency. These digital signals are sent to the top wakeup controller (top WUC), which coordinates communication with the microprocessor. The microprocessor receives signals from the top wakeup controller and responds by issuing commands to the top wakeup controller. The top wakeup controller determines what data to transmit (Tx$_0$, Tx$_1$) and enables the transmitter (Tx$_{EN}$) to send medical data to the external wand.

The transceiver uses a dual-resonator LC tank [47]. The dual-resonator allows higher frequency separation between the FSK tones compared to a single LC tank using a varactor. Using two separate bands completely eliminates the overlap between their phase noise skirts, thus relaxing oscillator phase noise requirements. It is formed by the series connection of two LC tanks (L$_0$C$_0$, L$_1$C$_1$) that are tuned to 433 MHz and 915 MHz. It resonates when a wireless signal at either of these frequencies is sent to the IOP monitor, with the ac signal developed across the corresponding LC tank. Therefore, the receiver can detect two wakeup signals to initiate separate microprocessor procedures or program the IOP monitor. Differential analysis of the received ac signals reduces the false wakeup rate from noise

outside of the resonance frequencies because those frequencies generate a common mode at the comparator input. Most importantly, DC outputs of the rectifiers, are cancelled out during this process. The dual-resonator transmits data by shorting one LC tank, enabling the oscillator, and radiating power from the inductor coils. It achieves high tone separation with 10% lower circuit area than two separate LC oscillators.

Wireless wakeup signals are detected by rectifying ac signals that are coupled onto the dual resonator. The ac signals are converted to a dc voltage using 8 full-bridge rectifier stages. Each half of the dual resonator is ac coupled to each of its associated rectifier stages, where Schottky diodes generate a dc potential. The Schottky rectifier is passive and has a smaller forward-bias voltage than diode-connected MOS transistors (200 mV vs. 450 mV for HVT NMOS devices in this technology), making it a suitable choice for this application. The passive nature of the Schottky rectifier enables us to cascade 8 stages to achieve a higher DC output without consuming the limited energy available to IOPM. The tradeoff in adding multiple stages is an increased output rise time from 80 $\mu$s (single stage) to 1.2 ms (8-stage), which is not important in this application as the external wakeup device will be held close to the IOPM for several seconds during transmission. The output of the 8-stage rectifier is converted to a full swing digital signal using a clocked comparator. This comparator runs continuously in standby mode, so it must be low power to meet the microsystem's energy budget. The comparator runs with a 31 pW 50 Hz clock that is generated at 0.45 V using a leakage-based oscillator [48] and then level-converted to the 3.6 V comparator input.

The transmitter uses an architecture that combines the local oscillator (LO) and power amplifier (PA). This modification is necessary to reduce circuit area by including fewer fully-integrated inductors. For PA functionality, the inductors need to be large to radiate enough power for the external wand to detect. However, the 0.41 mm diameter, 5-turn coils degrade LO phase noise because of low quality factor (Q). The Q of the inductors is further degraded by placing solar cells underneath the coil openings to save area. Based on 3D EM simulation results, inductor Q is reduced from 11 to 9.5 at 433 MHz, and from 12.3 to 10.6 at 915 MHz when solar cells were added. The effects of lower Q on phase noise are mitigated by using the dual-resonator with high frequency separation between tones.

During data transmission, the transceiver requires greater peak power than the battery can supply. Therefore the transceiver draws instantaneous power from a local charge reservoir. The local charge storage is implemented as 1.6 nF of integrated metal oxide semiconductor (MOS) and MIM capacitance on the ICs. The MIM density is 2 ff/$\mu$m$^2$ in this technology. The 1.6 nF value was the maximum amount of capacitance that could fit on silicon without violating our area constraint in Table I. The transceiver sends a single 100 ns pulse at a time, which degrades the voltage on the local supply by less than 25%. The local supply is then recharged for the next 131 $\mu$s from the battery, using a resistor to prevent high currents from damaging the battery, resulting in an effective data rate of 7.5 kb/sec (Fig. 8). Low-leakage IO devices with reduced sizes limit leakage power while meeting performance targets. The transmitter can send daily IOP data taken every 15 minutes in 130 ms.
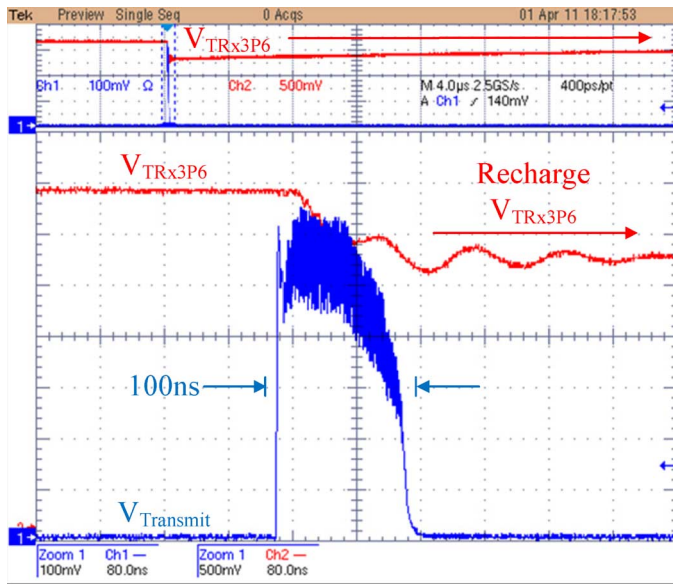
Fig. 8. Data transmissions are sent in 100 ns pulses because of peak power constraints.
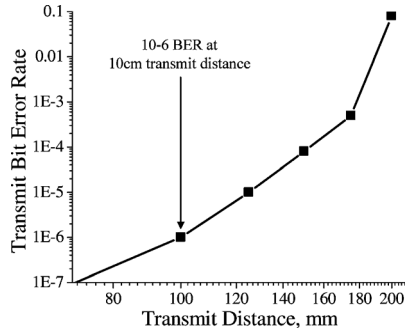


Fig. 9. Transmitter BER plot.



Fig. 10. (a) In-vivo radio testing implantation. (b) Measurement setup. (c) Received pulses at 433 MHz.

## C. Transceiver Measured Results

The transceiver is tested in a laboratory using an external wand to communicate with the IOPM. The wand contains PCB-trace inductors and matching networks connected to an RF signal generator and spectrum analyzer to transmit and receive data [49]. The transmit media between the IOP monitor and wand is air as well as 0.5 mm of saline to model the aqueous humor and cornea. The IOP monitor is demonstrated to wake up when a 1 W wireless signal is sent at a distance of 4 mm. After receiving this signal, the IOP monitor will respond by transmitting data to the wand with a BER of $10^{-6}$ at a distance of 10 cm. The transmit BER vs. transmission distance is shown in Fig. 9.

In order to demonstrate in vivo system operation, the radio was implanted in a mouse as shown in Fig. 10(a). The external wand [shown in Fig. 10(b)] receives the signal using a PCB coil. The received signal is amplified, filtered, and down-converted using a spectrum analyzer to reconstruct the transmitted waveform. Fig. 10(c) shows the successful reception of transmitted data in the implanted system.

## V. POWER MANAGEMENT AND ENERGY AUTONOMY

### A. Power Management Unit Background

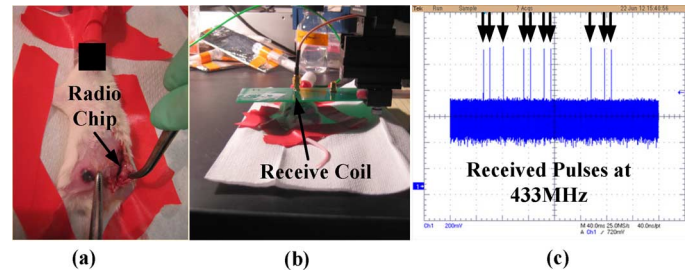Efficient energy harvesting and voltage regulation is necessary for energy-autonomous operation. Environmental energy

is sporadic and must be stored on a secondary supply for continuous power. Solar cells output below 500 mV [50] and secondary supplies commonly have higher voltages because of energy density or battery chemistry constraints, requiring dc-dc voltage conversion. Converter efficiency degrades at low loads because overheads do not scale down proportionally to delivered power. A low-power energy harvesting boost converter demonstrates 80% efficiency with a 100 $\mu$W harvester and 45% at 1 $\mu$W [51]. However, boost converters require large external inductors that do not meet the IOPM volume constraints. Switched capacitor voltage harvesters can be designed to perform dc-dc conversion using integrated capacitors. Harvesting switched capacitor networks achieve 84% efficiency at 1 mW [52] and 40% at 958 nW [33].

Energy stored on the secondary battery must be converted to the load circuit voltage levels. A buck-converter demonstrates 80% efficiency at a 1 $\mu$W load [53]. As with energy harvesting boost converters, buck-converters require external inductors which are too large for the IOP monitor, and switched capacitor voltage regulators achieve similar functionality with integrated capacitors. A down-converting switched capacitor voltage regulator achieves approximately 76% efficiency at a 100 $\mu$W load and 60% at 1 $\mu$W [29]. Linear regulators exhibit high line regulation and low output noise, but suffer from poor efficiencies at high conversion ratios and cannot be reused for energy harvesting. Hybrid switched capacitor plus linear regulator systems increase efficiency by reducing linear regulator dropout in systems with high conversion ratios. Hybrid dc-dc converters demonstrate efficiencies of 55% at 126 nW [48] and 18% at 100 pW [33].

### B. Power Management Unit Implementation

The power management unit recharges the battery from the solar cell and delivers power to load circuits (Fig. 11). The same switched cap voltage regulator (SCVR) that up-converts solar cell voltage to battery voltage is re-used to down-convert battery voltage and supply CMOS circuits. The solar cell size is limited to 0.07 mm$^2$ by the size restrictions of the monitor and is fabricated in an unmodified CMOS process, i.e., without any extra fabrication steps, using the deep n-well to p-well and p-well to n-active diodes. It is located underneath the transparent transceiver coil openings to save area. The output of the solar cell ($V_{\mathrm{SOLAR}}$) connects to the $V_{\mathrm{0P45}}$ node of the switched capacitor voltage regulator. When $V_{\mathrm{SOLAR}}$ exceeds 450 mV, the 0.32 mm$^2$ 8:1 voltage regulator up-converts the harvested energy to above 3.6 V and recharges the battery. The thin-film solid-state Li battery is supplied by Cymbet Corporation and uses a commercial chemistry, but its size is tailored specifically for this application [54]. This tailoring is necessary since most commercial

Fig. 11. The switched capacitor voltage regulator up-converts solar energy to power the capacitance to digital converter and transceiver, and also recharge the battery. It down-converts stored energy to supply power to digital circuits when there is no solar energy.



Fig. 12. The 0.32 $\text{mm}^2$ 8:1 switched capacitor voltage regulator uses minimum-sized power switches and reduced swing clocks to reduce switching overhead.

batteries are designed at mA-hr range capacities with dimensions much bigger than IOPM dimensions to achieve sub-k$\Omega$ internal resistance [55]. The custom battery used in IOPM meets the volume constraint at the cost of reduced current driving ability (only 10 $\mu$A at 3 V). As mentioned in Section IV, the limited battery peak current problem is alleviated by running the transmitter off storage capacitors during radio transmission. Also, since lowering the battery voltage below 3 V would significantly degrade its capacity, radio transmissions are made shorter (100 ns as shown in Fig. 8) to avoid capacity loss.

$V_{0P45}$ also supplies the microprocessor and SRAM, allowing the solar cell to directly power the load circuits. When the open-circuit solar cell voltage drops below $V_{0P45}$, the solar cell acts as a load to the microsystem and is disconnected. The open circuit voltage is detected using a small replica solar cell. When $V_{0P45}$ drops below 0.45 V, power is down-converted from the battery by the same switched capacitor voltage regulator used for energy harvesting and delivered to the load circuits. Voltage comparisons in the power management unit are performed with clocked comparators that are switched by the SCVR and top wakeup controller clocks.

The switched capacitor voltage regulator uses an 8:1 ladder topology to perform dc-dc voltage up and down conversion (Fig. 12). The ladder contains dc nodes at 450 mV intervals, and transfers charge up and down the ladder between adjacent nodes. Eight 35 fF MOS capacitors store charge on the dc nodes. The storage caps are sized to minimize ripple at these nodes while maintaining reasonable area. MOS capacitors achieve higher density, and their parasitics have little effect on switched capacitor voltage regulator performance since the voltages on these capacitor terminals do not change. Seven 45 pF MIM capacitors transfer charge between the dc nodes and are located on top of the MOS caps in the physical design. These capacitor values are chosen to be sufficiently large to meet microsystem load power requirements while minimizing capacitor area. The voltages on these capacitor terminals change when the switched capacitor voltage regulator is clocked, so MIM capacitors are used to reduce parasitic bottom plate capacitance.

Switching losses dominate conductive losses at the IOP monitor's low power levels, so clock load and voltage swing is minimized to increase efficiency. The power switches are minimum sized IO devices. NMOS switches are used except for the highest voltage portions of the ladder, where PMOS devices are used to increase overdrive. The ladder topology requires a high voltage supply to power the switches. Hence, the battery must have an initial minimal voltage for the microsystem to operate and to harvest energy. The 100 kHz clock is generated at 0.9 V from an internal node, level converted to 1.8 V clocks with dc offsets of 0 V, 0.9 V, and 1.8 V, and used to drive the power switches. The clock voltage swing was optimally chosen to improve efficiency. Higher clock swings increase switching energy, while lower clock swings degrade performance by weakening power switches. The dc voltage levels are chosen to fully turn off each power switch. Level conversion is performed with differential cascade voltage switch (DCVS) gates that are supplied from internal SCVR nodes.

### C. Power Management Unit Measured Results

The power management unit is tailored for the microsystem's power sources and loads to maximize lifetime. With IOP measurements every 15 minutes, 10,000 microprocessor cycles for DSP per measurement, and daily transmission of 14 b raw IOP data, the average microsystem power is 5.3 nW (Table II). Standby transceiver leakage and active capacitance to digital converter power dominate the microsystem's energy requirements. The transmitter uses large devices in the combined LO and PA to transmit sufficient power for the external wand to detect. These 192 $\mu$m devices have 3.3 nW leakage in standby mode even though they are implemented as low-leakage IO devices. The capacitance to digital converter requires 10 000 cycles to achieve the target IOP accuracy of 0.5 mmHg, setting the capacitance to digital converter energy per measurement. Digital components make smaller contributions to IOP monitor energy usage. Fig. 13 shows the efficiency of switched capacitor network when down-converting from 3.6 V to 0.45 V at different current loads. In active mode, the switched capacitor voltage regulator delivers power from the 3.6 V battery to the 90 nW 0.45 V microprocessor, SRAM, and wakeup controllers with 75% efficiency. In standby mode, it delivers 72 pW with 40% efficiency. A performance summary comparing this design to demonstrated previous works in energy harvesting and voltage regulation is shown in Table III.

The IOP monitor achieves energy autonomy by harvesting more energy than it requires for operation. In sunlight with a light irradiance of 100 $\text{mW}/\text{cm}^2$ AM 1.5 [56], $V_{\text{SOLAR}}$ reaches 500 mV, and 80 nW is delivered to recharge the battery (Fig. 14).
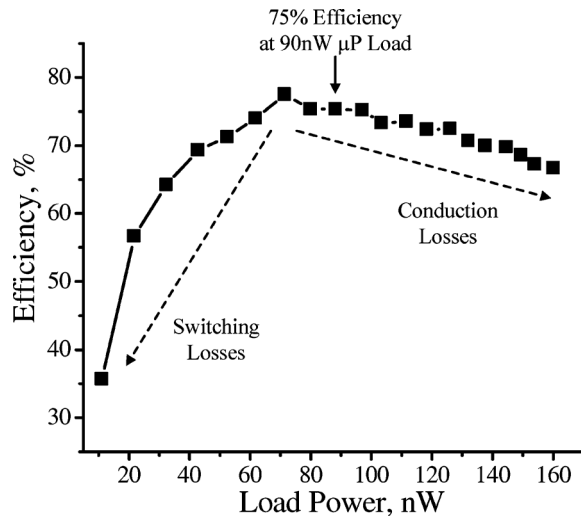
Fig. 13. The switched capacitor voltage regulator is optimized for low switching and conduction losses to achieve 75% efficiency.

TABLE II
POWER BREAKDOWN FOR THE IOPM

| Active Mode | Power | Time/Day | Energy/Day |
|---|---|---|---|
| CDC | 7.0 µW | 19.2 s | 134.8 µJ |
| TRx | 47.0 mW | 134.4 µs | 6.3 µJ |
| SCVR | 116.9[a] nW | 19.2 s | 2.2 µJ |
| ● µP+SRAM | 90.0 nW | 19.2 s | 1.7 µJ |

| Standby Mode | Power | Time/Day | Energy/Day |
|---|---|---|---|
| CDC | 172.8 pW | 24 hr | 14.9 µJ |
| TRx | 3.3 nW | 24 hr | 285.1 µJ |
| SCVR | 174.8[b] pW | 24 hr | 15.1 µJ |
| ● µP+SRAM | 9.8 pW | 24 hr | 846.7 nJ |
| ● WUC | 62.0 pW | 24 hr | 5.2 µJ |

[a]Includes µP and SRAM power
[b]Includes µP, SRAM, and WUC power

While these conditions are not typical, in indoor lighting with light irradiance of 15 $\mu$W/cm$^2$, $V_{SOLAR}$ drops to near 460 mV and the battery is still recharged with 13 nW, more than offsetting the 5.3 nW monitor's power consumption. The IOPM requires 10 hours of indoor lighting or 1.5 hours of sunlight per day to achieve energy-autonomy. In the latter scenario, the 459 $\mu$J energy required by the microsystem is harvested in 1.5 hours at a rate of 80 nW. Energy-autonomy makes the IOP monitor lifetime decades or longer, giving doctor's ample time tailor a patient-specific glaucoma treatment.

## VI. CONCLUSION

A 1.5 mm$^3$ microsystem, targeted for minimally invasive implantation, measures IOP with an accuracy of 0.5 mmHg. Based on in vivo measurements, the transmitter wirelessly transmits measured pressure data through animal tissue to an external wand. It is designed to transmit data from within the eye to an external wand while consuming 4.7 nJ/bit, providing rapid IOP feedback to decrease physician response time for improved treatment. It harvests up to 80 nW of solar power in

TABLE III
PERFORMANCE SUMMARY OF PREVIOUS WORKS IN DC-DC VOLTAGE
CONVERSION

| Reference | Method | Efficiency | Power | $V_{IN}$ | $V_{OUT}$ |
|---|---|---|---|---|---|
| **This Work** | SCVR | 75% | 90nW | 3.6V | 450mV |
| **This Work** | SCVR | 40% | 72pW | 3.6V | 450mV |
| [57] | SC-CP | 60% | 1.2mW | 80mV | 500mV |
| [51] | Boost | 80% | 100µW | 250mV | 1V |
| [51] | Boost | 45% | 1µW | 250mV | 1V |
| [52] | SCVR | 84% | 1mW | 1.15V | 2.1V |
| [52] | SCVR | 10% | 1µW | 1.15V | 2.1V |
| [33] | SCVR | 40% | 958nW | 865mV | 3.6V |
| [53] | Buck | 80% | 1µW | 1.2V | 500mV |
| [29] | SCVR | 76% | 100µW | 1.2V | 500mV |
| [29] | SCVR | 60% | 1µW | 1.2V | 500mV |
| [48] | Hybrid | 55% | 126nW | 3.6V | 444mV |
| [33] | Hybrid | 41% | 100nW | 3.6V | 400mV |
| [33] | Hybrid | 18% | 100pW | 3.6V | 400mV |



Fig. 14. The solar cells and switched capacitor voltage regulator deliver of power to recharge the battery.

sunlight with a light irradiance of 100 mW/cm$^2$ AM 1.5 and uses ultra-low-power circuit techniques to achieve energy autonomy, extending lifetime indefinitely and potentially giving doctors time to converge upon the best glaucoma treatment. Energy-autonomous and nanowatt circuit techniques are needed to the enable cubic-millimeter microsystems that could eventually be used as part of future medical implants, such as blood pressure and glucose sensors, as well as non-medical devices, such as supply chain and infrastructure monitors.

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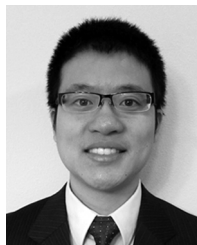
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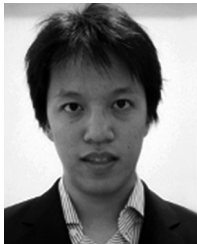
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