Increased Blocking Voltage in Solution Processed ZTO HVTFTs through Drain Offset

MICHIGAN ENGINEERING
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Motivation

- Heterointegration of thin film power electronics for "electronics on anything"
- Goal of this work: Solution-processed ZTO HVTFTs for 100-200V with reasonable on-current and high ON/OFF ratio

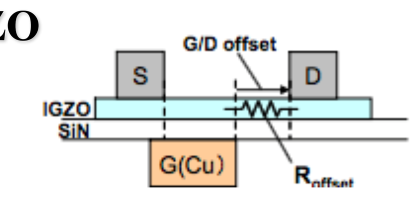
Amorphous Oxide Semiconductors for Power

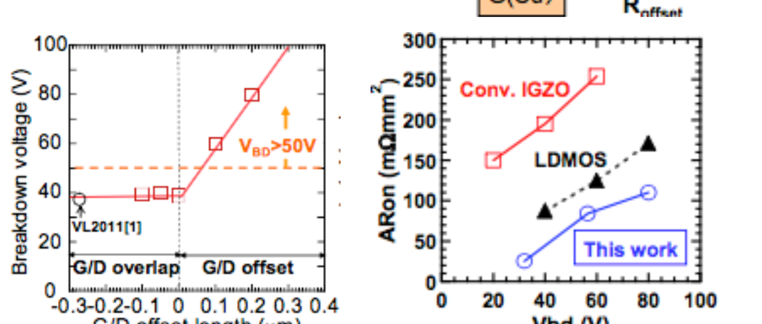
Comparison of semiconductor properties (yellow = advantages of AOS)

Property (at 300K)	SiC	ZnO	AOS	GaN
Crystalline structure	wurtzite	wurtzite	amorphous	wurtzite
Bandgap (eV)	3.23 (D)	3.3 (D)	3.3 (D)	3.4 (D)
Relative dielectric constant	9.66	8.75	11.5-13.8	10.6
Electron mobility (cm²/V-s)	< 900	226	10-30	5300
Breakdown e-field (kV/cm)	~ 1000	> 100-300**	*	2,600
Cost / process complexity	High	Low	Low	High

***Little or no experimental data available; **Breakdown in poly-ZnO occurs along grain boundaries.**

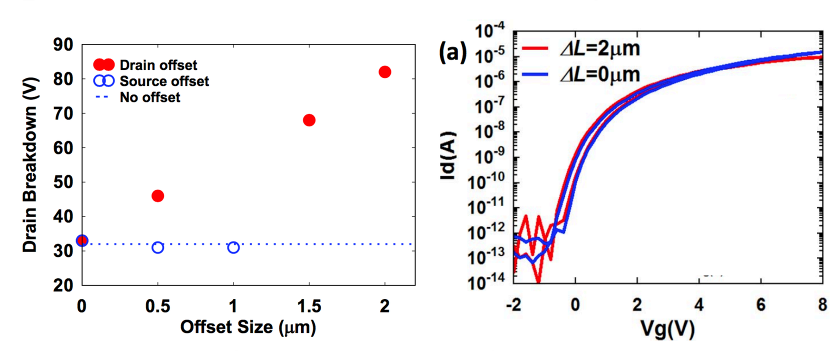
- **Sputtered IGZO**
  - **Desire indium free material**





H. Sunamura et al., Symp. on VLSI Technology, 2014, pp. 1–2.
K. Kaneko et al., Symp. on VLSI Technology, 2012, pp. 123–124.

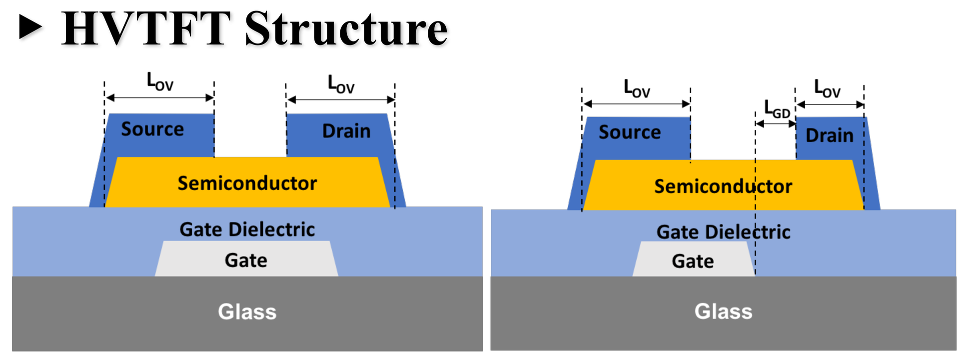
- **Transparent amorphous oxide semiconductors**
  - AOS offers wide bandgap and large dielectric constant
  - High quality films obtained through solution or vacuum deposition; no need for bulk crystals
- **Nano-crys. ZnO**
  - **Desire solution processed material**

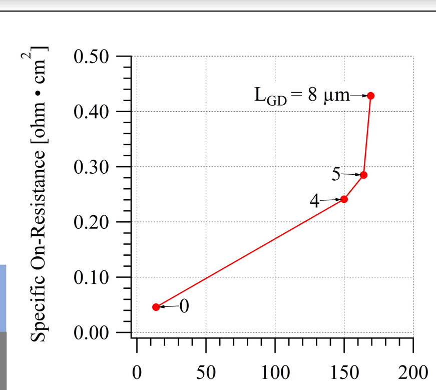


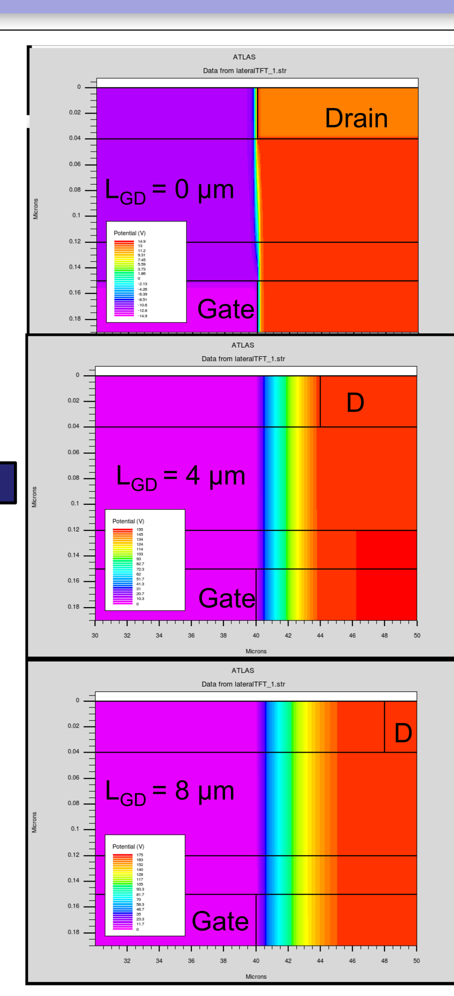
Gong and Jackson, DRC 2016

Device Fabrication

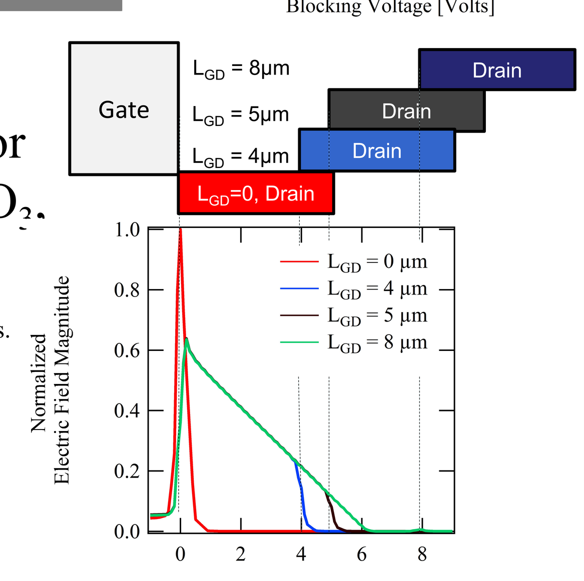
- **HVTFT Structure**





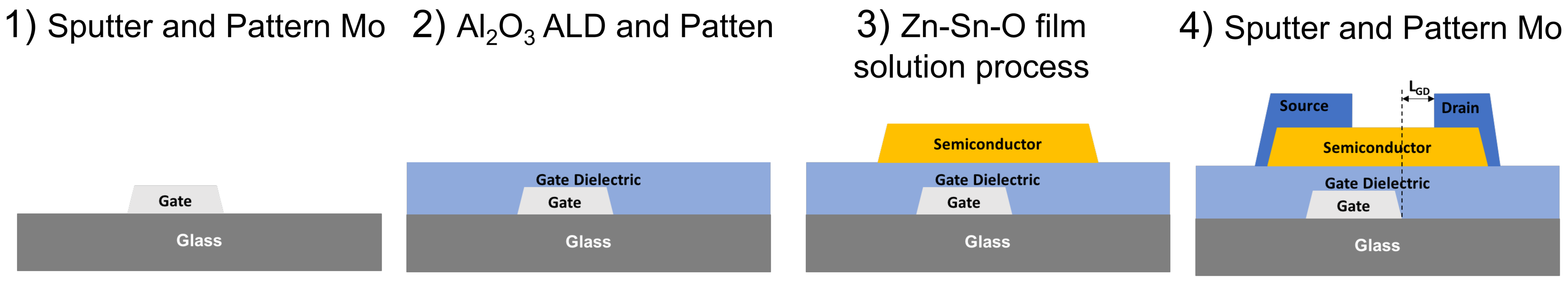


- Drain offset distributes electric field
- Used in a wide variety of semiconductor transistors with GaN, Si LDMOS, Ga_2O_3, SiC, etc.
- Used with a-Si TFTs in 1993 [Martin *et al.*, Trans. Electron Dev. 1993]

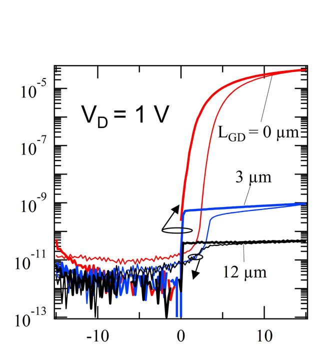


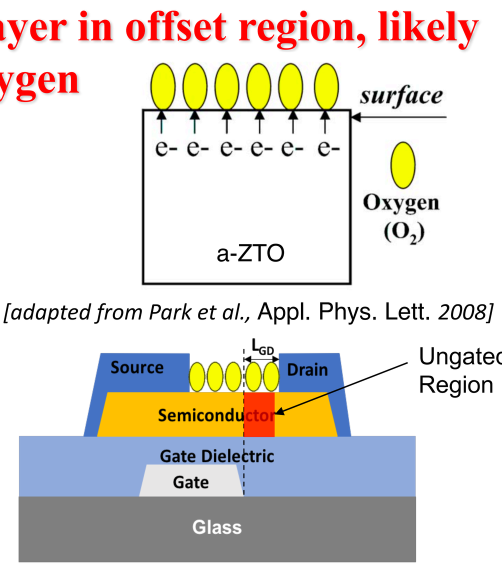
- **HVTFT Diode Fabrication**

1) Sputter and Pattern Mo 2) Al_2O_3 ALD and Patten 3) Zn-Sn-O film solution process 4) Sputter and Pattern Mo



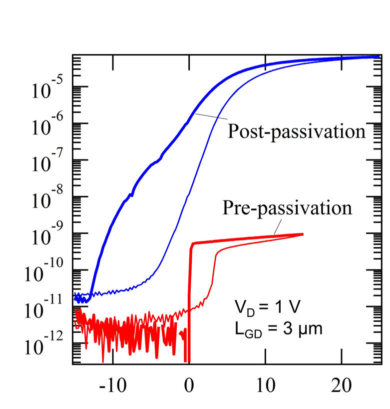
- **Large offset region resistance due to depletion of ZTO layer in offset region, likely due to absorbed oxygen**

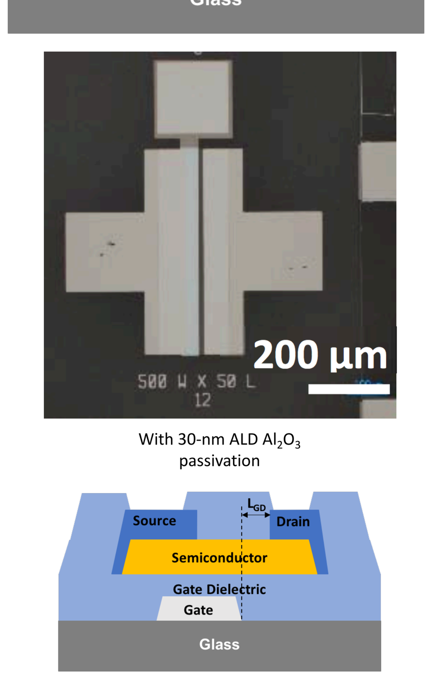




[adapted from Park *et al.*, Appl. Phys. Lett. 2008]

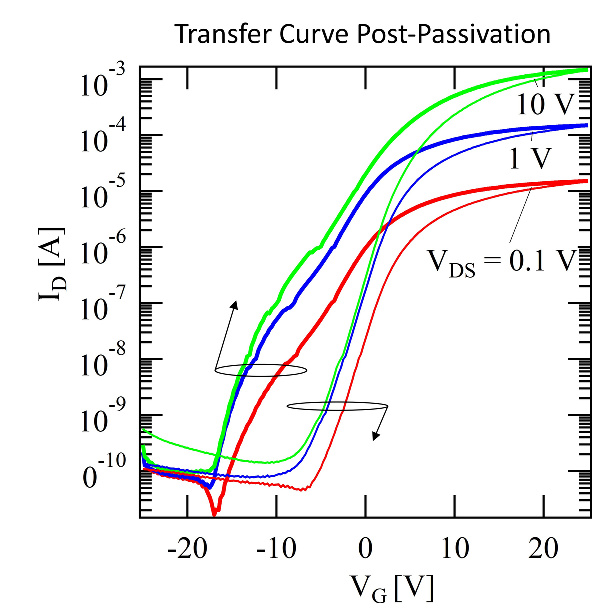
✓ **Passivation increases conduction**

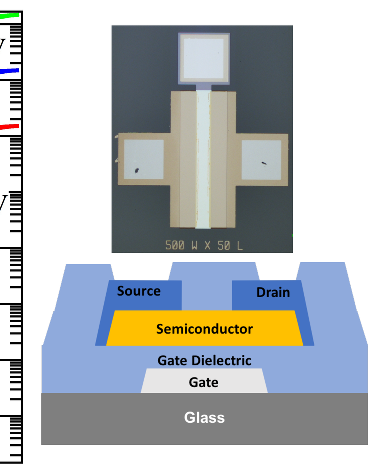




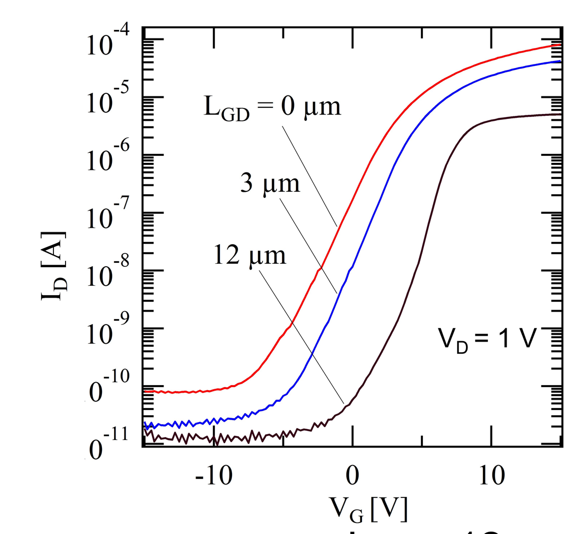
With 30-nm ALD Al_2O_3 passivation

Results and Discussions

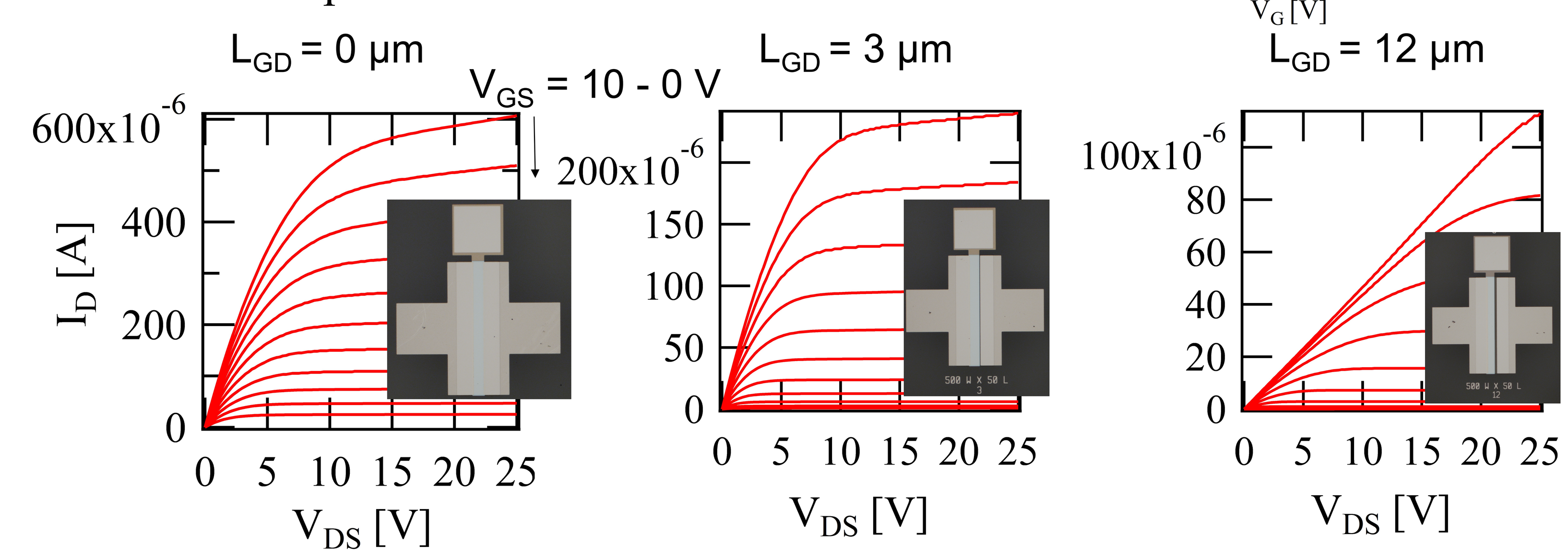




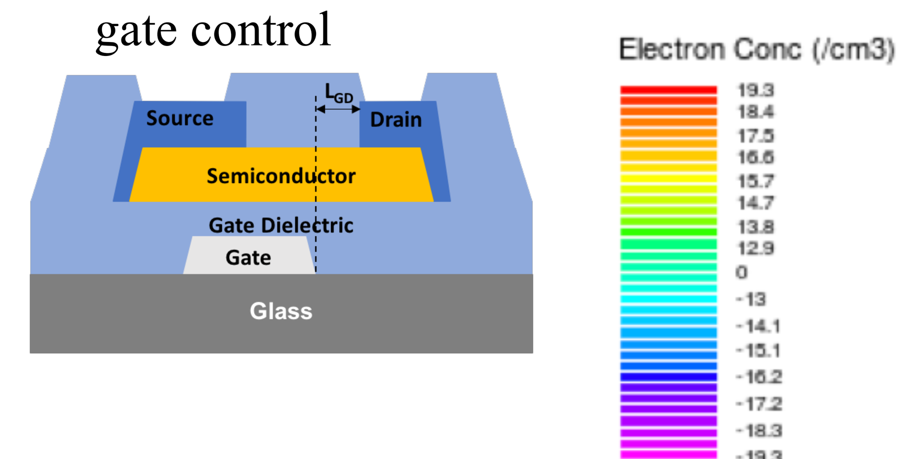
- **Performance of 0 μm offset device**
  - $\mu_{linear} = 11.8\ cm^2V^{-1}s^{-1}$
  - $C_{ox} = 72.3\ nF\cdot cm^{-2}$
  - $V_t = -0.4$ V
  - $I_{on}/I_{off} > 10^6$

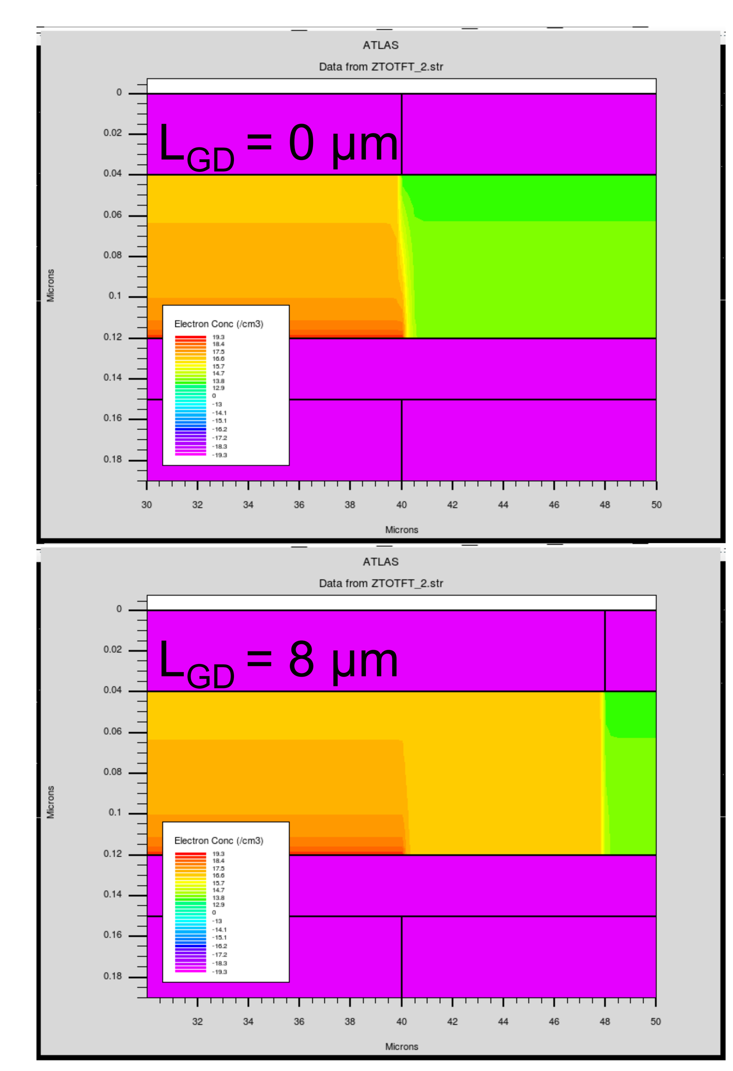


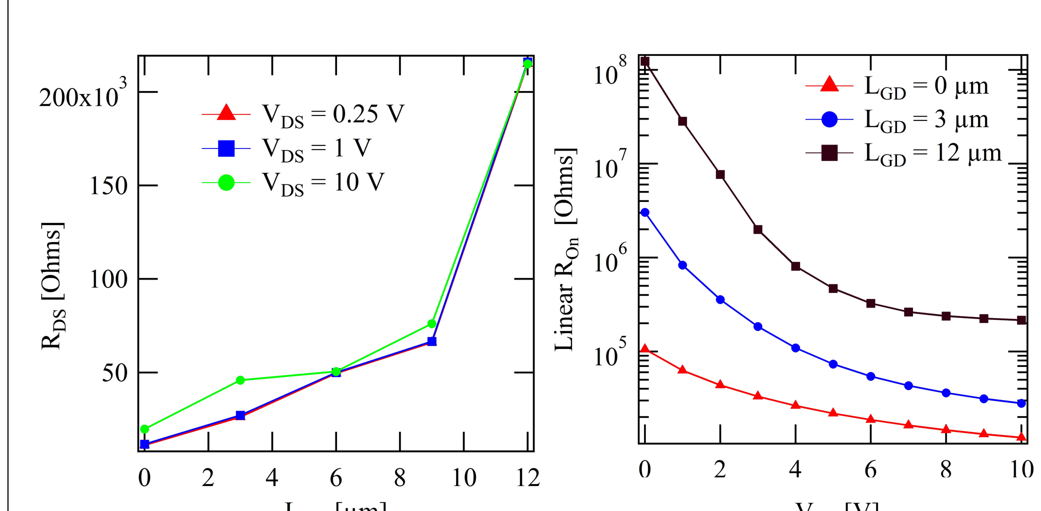
- **Offset electrical performance**
  - As drain offset length increases, on-current decreases and linear region in output curve becomes more prominent



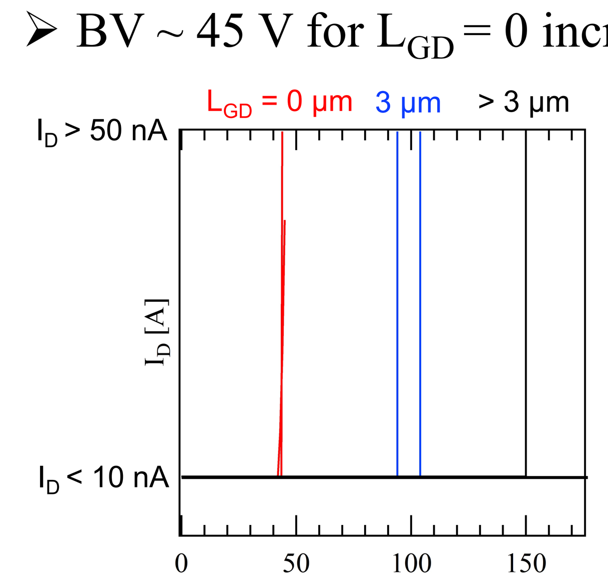
- **Increasing resistance with offset**
  - Increasing offset length increases region without gate control



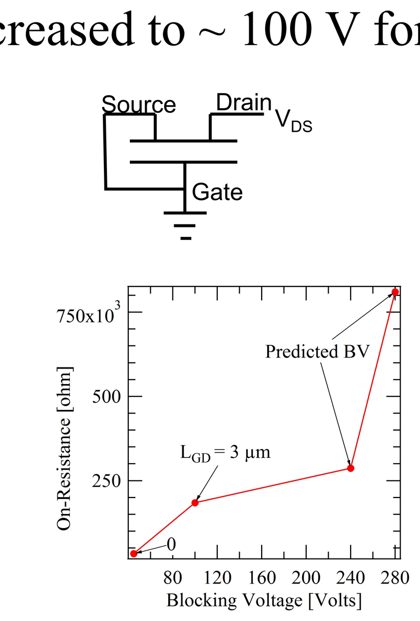


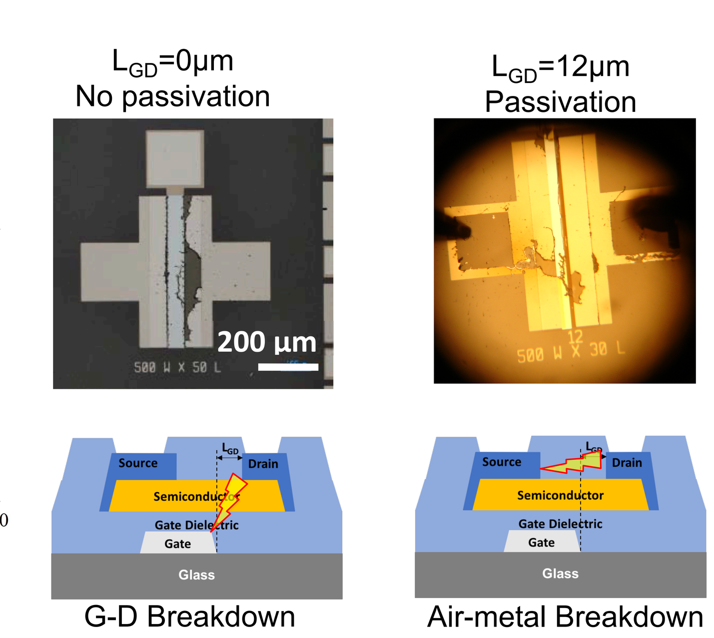


- **Source to drain breakdown**
  - BV ~ 45 V for L_{GD} = 0 increased to ~ 100 V for 3 μm offset



Current resolution limited by current setup





G-D Breakdown Air-metal Breakdown

Conclusion and Future Work

- Demonstrated solution-processed HVTFT with drain offset
  - ✓ 3 μm offset increases blocking voltage from 45 V to about 100 V
- Drain offset increases blocking voltage by improving electric field distribution but increases on-resistance
- **Future Goal**: Better field control for higher blocking voltage and lower on-resistance

Acknowledgements

- This work was supported by SPAWAR through DARPA Young Faculty Award N66001-14-1-4046. Any opinions, findings, conclusions or recommendations expressed in this publication are those of the authors and do not necessarily reflect the views of DARPA or SPAWAR.
- Thanks to Mr. Rodrigo Cuba for LabVIEW coding.

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