



A Non-Uniformly-Sampled Digital Controller for Constant-On-Time Valley-Current-Mode (NUS-COTCM) Buck Voltage Regulation Modules (VRMs)

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Motivation

- With the relentless pursuit for more powerful communications and microprocessors, the demand for VRMs that are faster, more accurate, and more flexible is inescapable.
- Some criteria for the choice of VRM controllers include fast response, straightforward control loop design, flexibility, low-complexity hardware, input disturbance rejection, and fast current-limiting [10].

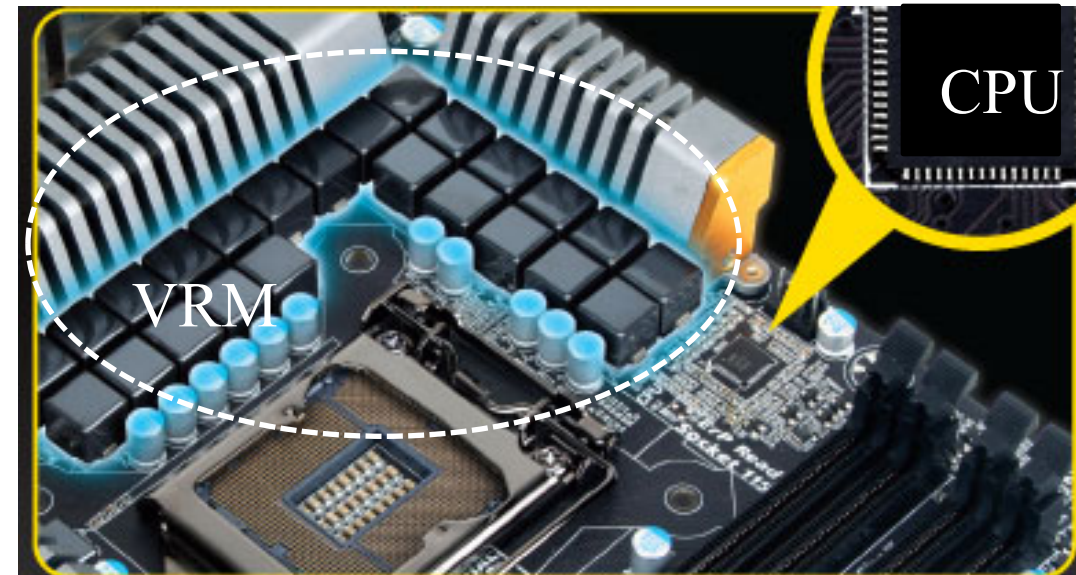


Fig. 0. VRM Examples

Method

Discrete Event Space Modeling:

The sampling action of the output voltage $V[n]$ is right before the turn-off transient. $I[n]$ the valley value of inductor current are not from the same physical time as $V[n]$, but in two discrete sequences that intersect each other.

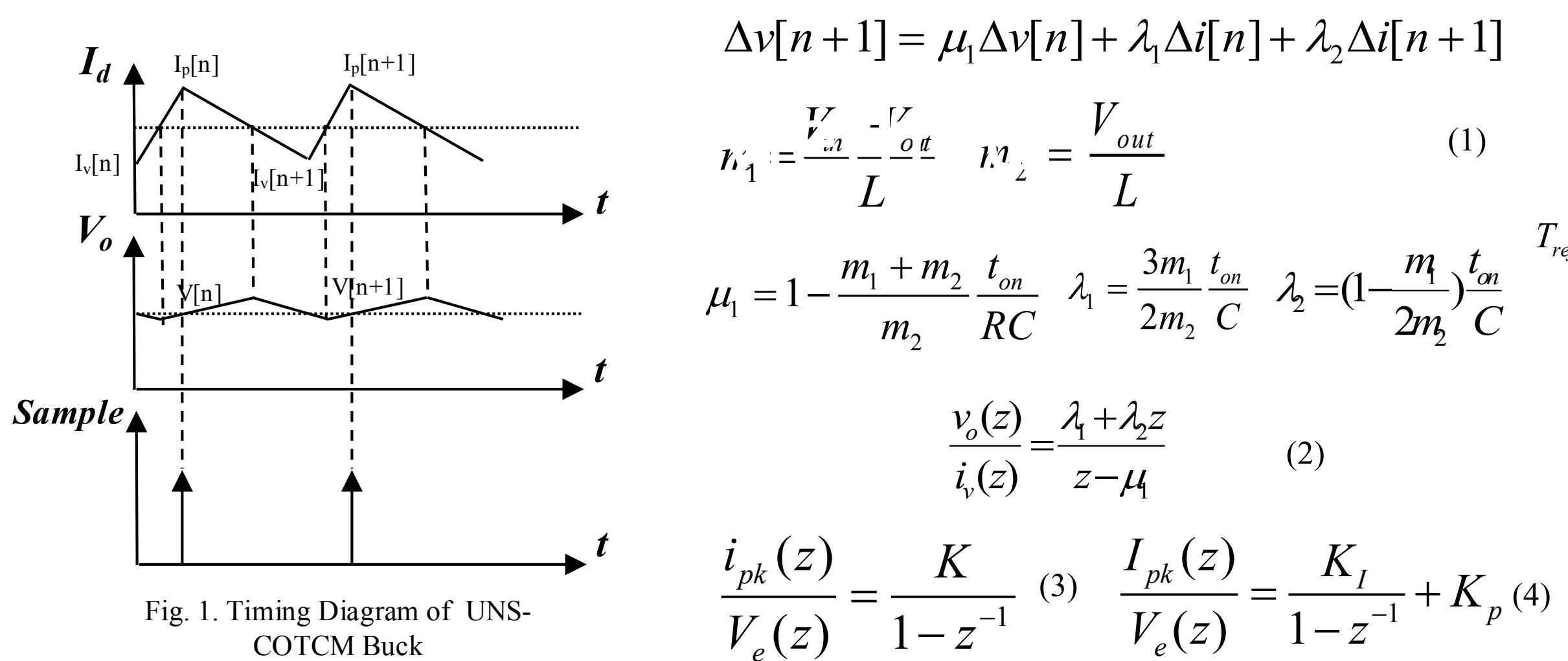


Fig. 1. Timing Diagram of UNS-COTCM Buck

The small-signal event space model is derived as (1) and the model's z-domain expression is shown in (2).

Compared to the single pole system in a peak-current-mode buck model [12], the discrete event-space buck model possibly has a non-minimum-phase zero, albeit far away from the pertinent dynamics.

Reference

- [10] D. Maksimovic and R. Zane, "Small-signal Discrete-time Modeling of Digitally Controlled DC-DC Converters," 2006 IEEE Workshops on Computers in Power Electronics, Troy, NY, 2006, pp. 231-235.
- [12] Cheng Hong, Wang Cong, Modeling, control and digital controller implementation of switching power converters. Tsinghua University Publisher, 2013.
- [13] N. Rathore and D. Fulwani, "Event triggered control scheme for power converters," IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 1342-1347.
- [14] R. Redl and I. Novak, "Instabilities in current-mode controlled switching voltage regulators," 1981 IEEE Power Electronics Specialists Conference, Boulder, Colorado, USA, 1981, pp. 17-28. doi: 10.1109/PESC.1981.7083621

Method

Control Architecture:

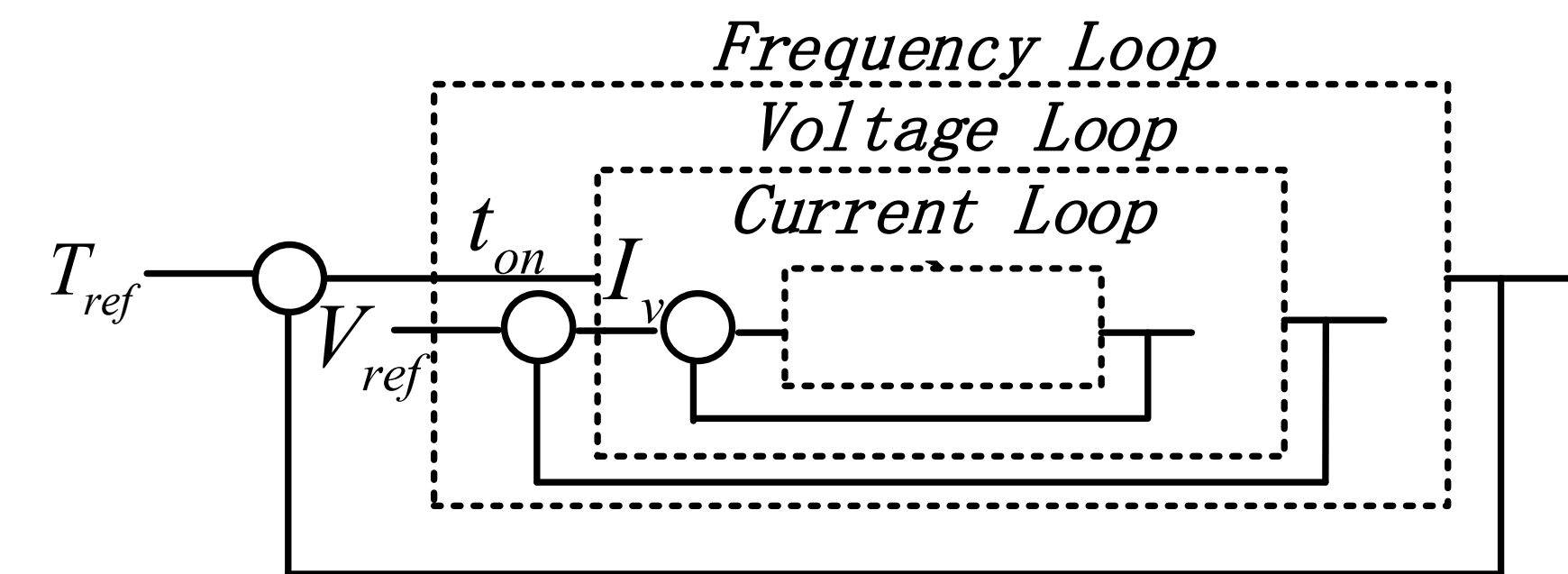


Fig. 2. Three Loops Control Structure

- The proposed control method includes three control loops (Fig 2). **Inner very fast analog current loop:** always settles in one cycle. **Outer slow digital frequency loop:** controlled on-time to achieve fixed switching frequency.

A fast digital voltage loop: with event-driven(ED) controller.

- Two event-driven controllers [13] for the voltage loop compensation are introduced; ED accumulators shown in (3) and ED proportional-plus-accumulators shown in (4).
- Control algorithms are implemented by DSP and control flows are shown in Figure 9.

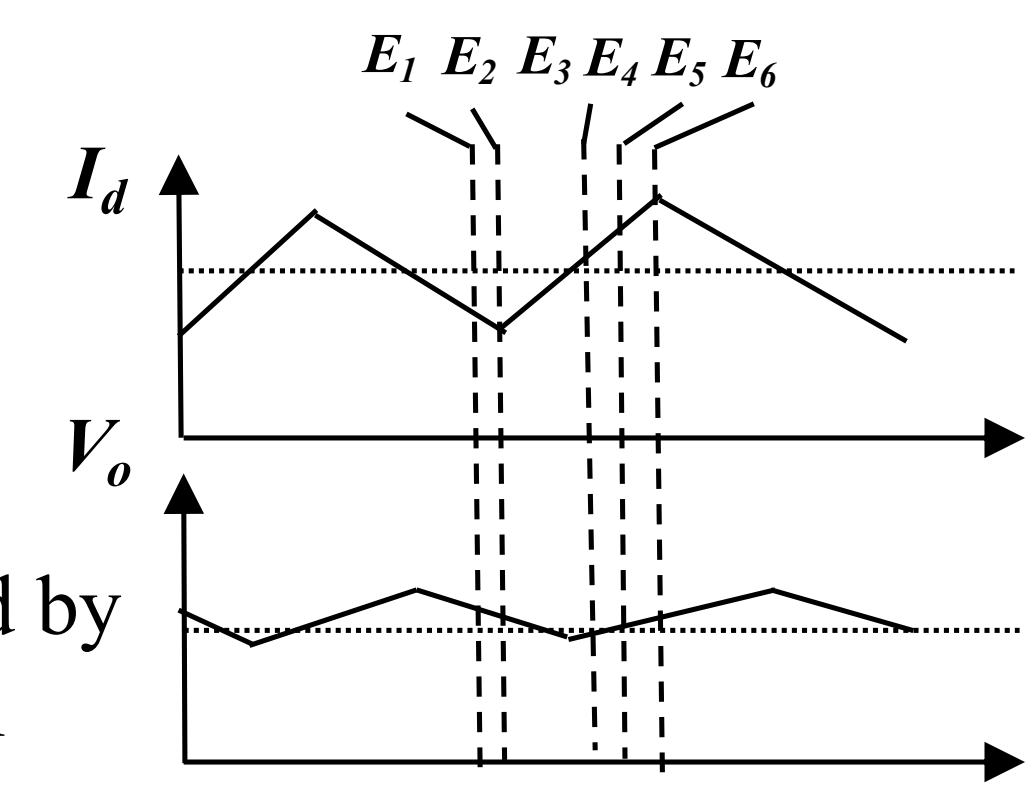


Fig. 9.1 Control Flow 1

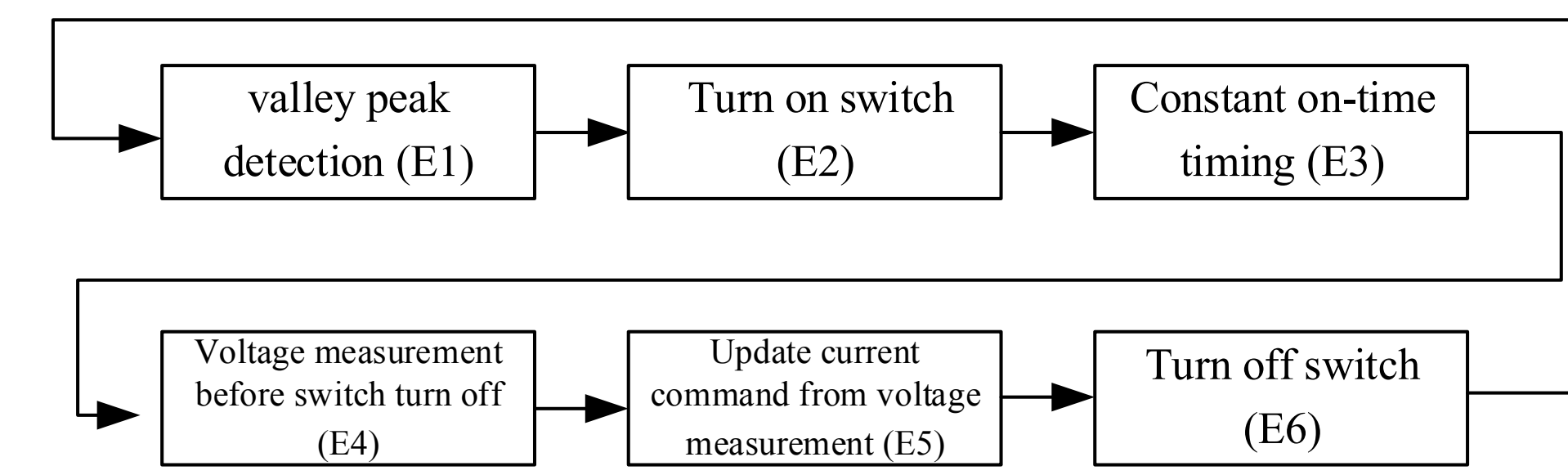


Fig. 9.2 Control Flow 2

Conclusion

- This paper introduces a new method for controlling Voltage Regulator Modules (VRMs) that potentially offers the fastest closed-loop transient response in comparison to existing methods.
- We present a new perspective in sampling where the sampling events are kept in phase with the switching events, which are in general non-periodic.
- Constant-on-time buck: light-load efficiency performance and in current mode, fast transient response.
- Digital controllers: control flexibility (e.g. nonlinear control), lower quiescent power, and robustness to component variations.
- Event synchronization: absence of intermodulation effects, very relaxed anti-aliasing filter, opportunity to avoid switching transients

Discussion

- In comparison, the controllers are designed to achieve the fastest step response with similar overshoot.
- C2: slow due to the anti-aliasing filter in the feedback loop, which is designed to attenuate the lowest switching frequency ripple.
- C3: aliasing of output voltage ripple (Fig. 5). Sampling frequency should be set much higher or much lower than the switching frequency
- C4: slope compensation required for D<0.5 operation[14]. Inner loop has a finite settling which degrades the response.

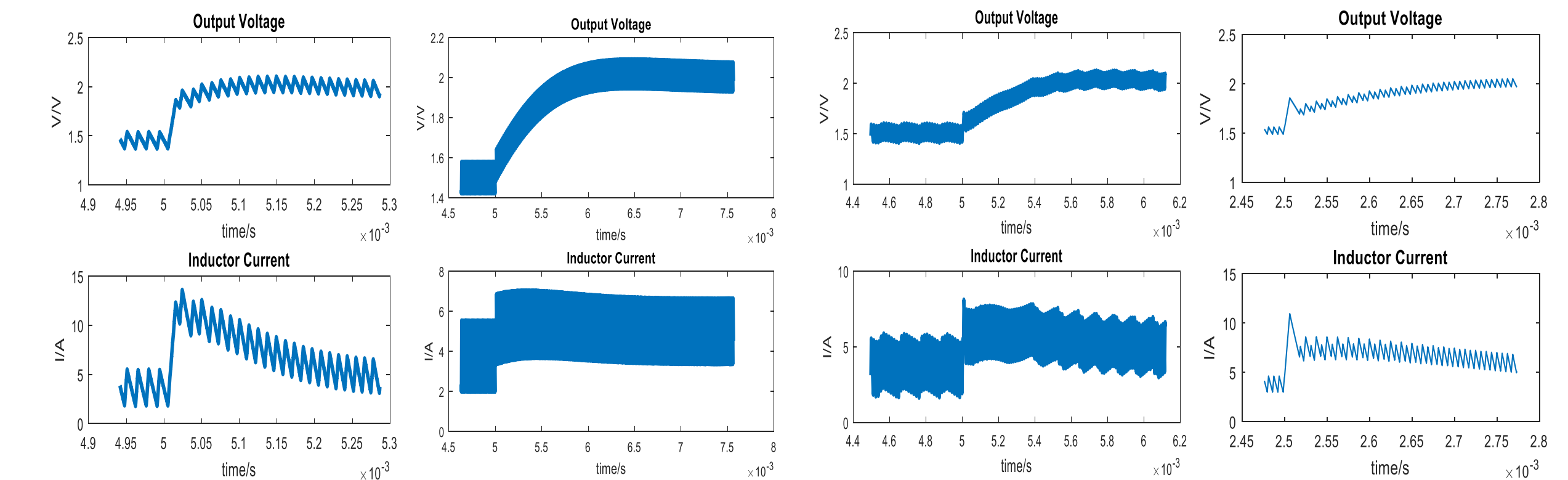


Fig. 3. NUS-COTCM Controller (C1)

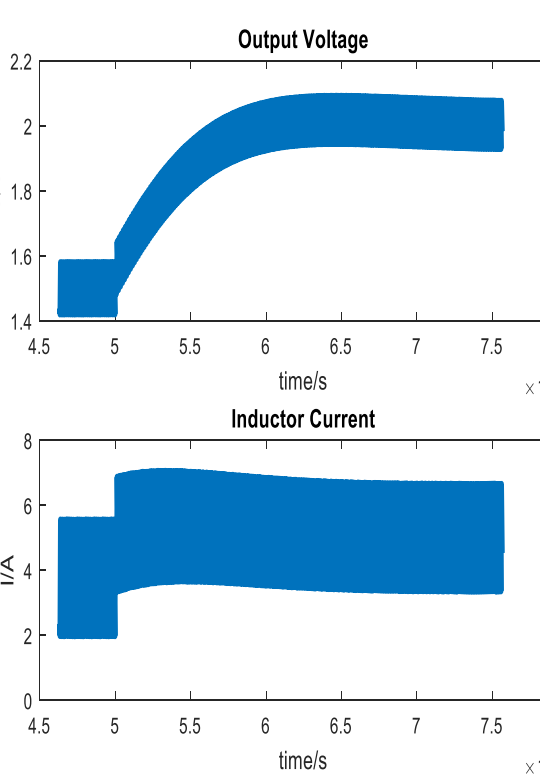


Fig. 4. Analog Constant-On-Time Current-Mode Controller (C2)

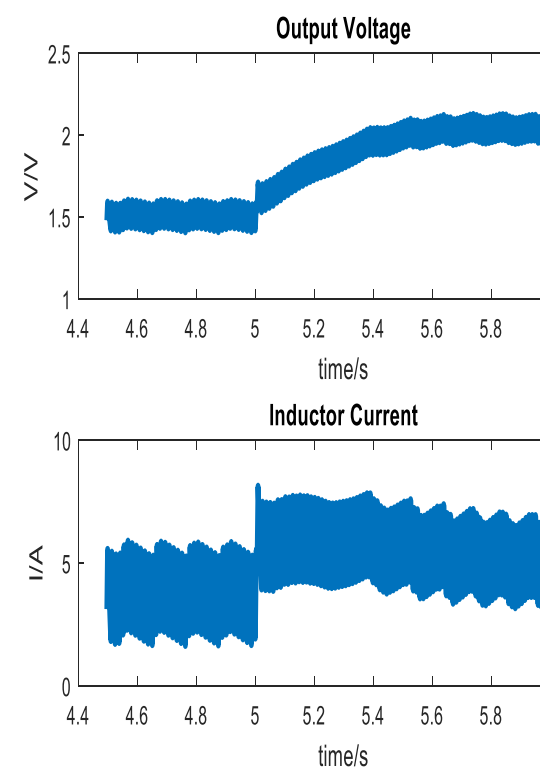


Fig. 5. Uniformly Sampled Digital Constant-On-Time Current-Mode Controller (C3)

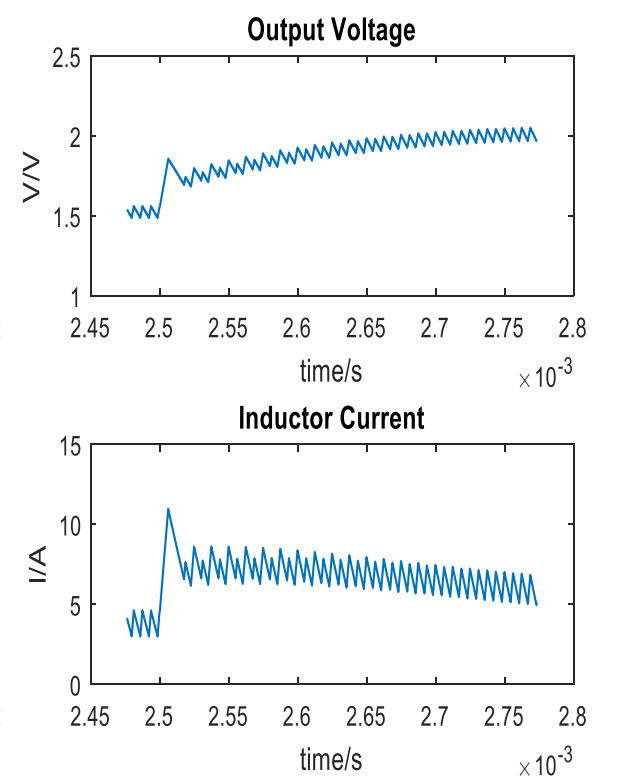


Fig. 6. Digital Fixed-Frequency Valley-Current-Mode Controller (C4)

Table 1. Comparison of VRM Controllers

Controllers	NUS-COTCM	Analog Constant-On-Time Current-Mode	Uniformly Sampled Digital Constant-On-Time Current-Mode	Digital Fixed-Frequency Valley-Current-Mode
Settling Time (μ s)	100	1000	500	200

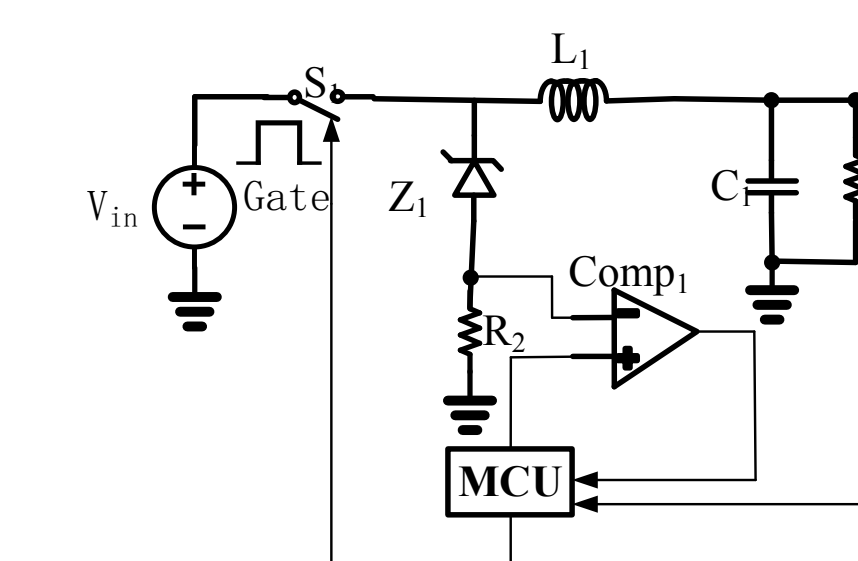


Fig. 7 Schematic for NUS-COTCM buck

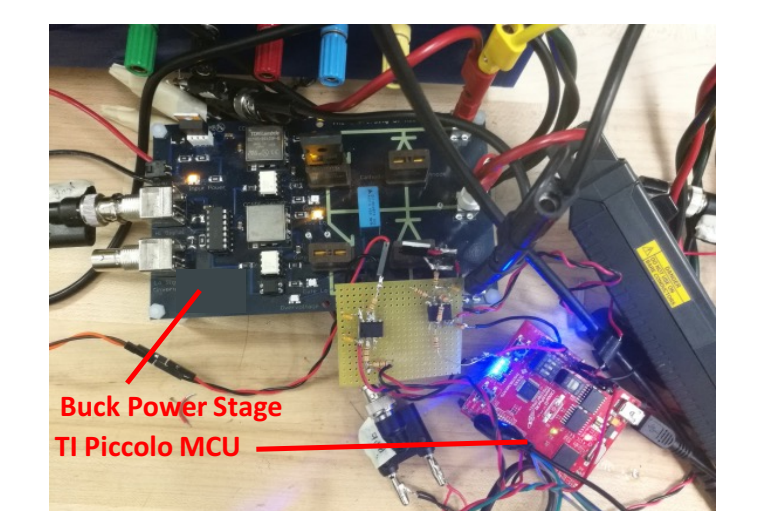


Fig. 8 Prototype of NUS-COTCM buck

- The corresponding small signal step-up-reference transient response in Fig. 10 and Fig. 11 settles in approximately 15 cycles.
- The rise time is about 60 μ s and settling time about 150 μ s, which is fast for a converter with a steady-state switching frequency of 100 kHz.
- The transient disturbance of the frequency loop with a 60 kHz reference is shown in Fig. 12. The loop slowly changes the on time towards a fixed steady-state frequency.

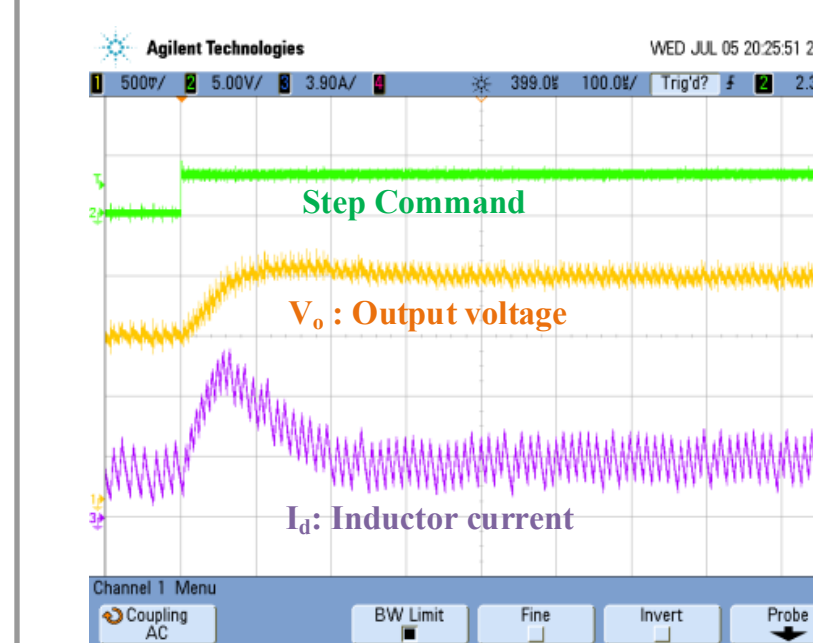


Fig. 10. Voltage loop small signal step response (zoom out)

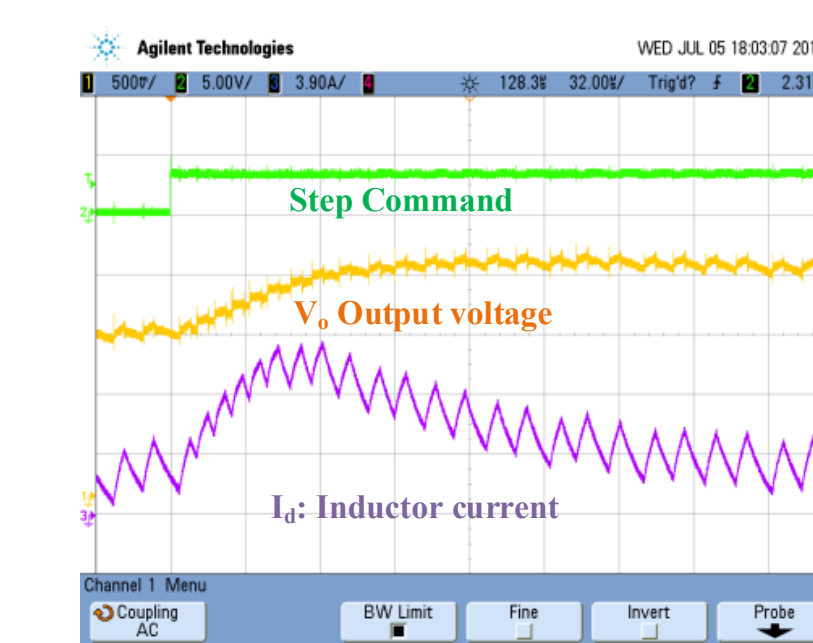


Fig. 11. Voltage loop small signal step response (zoom in)

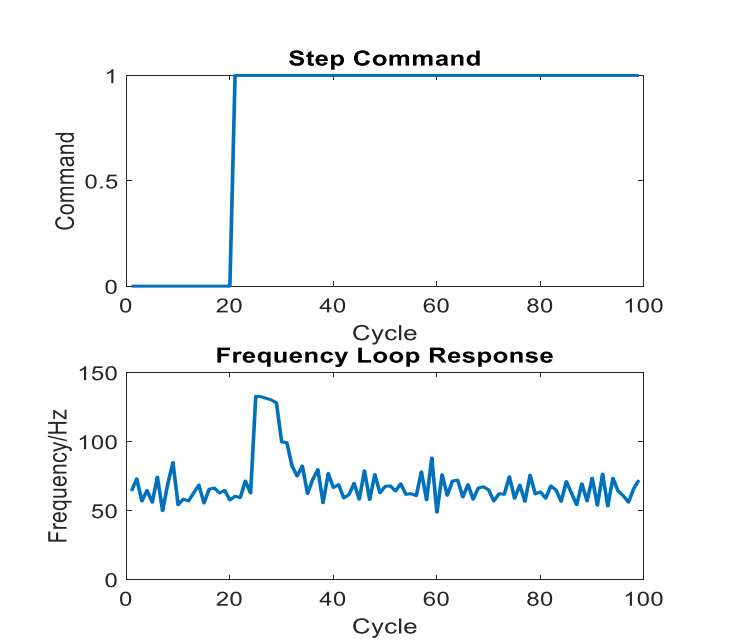


Fig. 12. Frequency loop step response