Sub-Millimeter Packages for Microsystems in Harsh Environment Applications

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Summary: Microsystems capable of sensing temperature, pressure and other parameters are needed for many applications, e.g., gathering information in downhole environments for oil and gas exploration. Certain target locations limit the size of the microsystems to sub-millimeter scale. In addition, the high temperature, high pressure, and corrosive ambient environments require special considerations. The size limitation and harsh factors in environments require sub-millimeter scale packages to protect sensing microsystems. The package needs to be made of mechanically and chemically robust materials, and bonding and assembly temperature must be low to allow the encapsulation of batteries.

The first generation of the system package was featured with sub-mm size (0.8x0.8x0.8 mm^3) and robust materials (stainless steel and glass/sapphire) [1]. Test chips were integrated using folded flexible cables and inserted in the packages. The packages were hermetically sealed using Au-In bond at 200ºC, and survived >48 h in 80ºC API brine (8 wt% NaCl & 2 wt% $CaCl_2$), followed by 50 MPa (7,250 psi) high pressure, without loss of hermeticity.

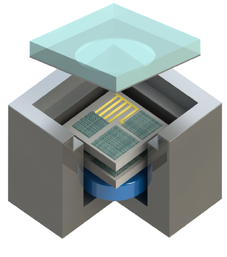
For the second generation of the system package, we introduced a new double-clamshell packaging approach that incorporates microcrimping [2]. It uses arrays of hollow structures, fabricated in hard steel and soft Al. The Al shells, which house the electronics, are inserted into the steel structures. Applied pressure causes the soft Al to undergo crimping, achieving the bond at room temperature. Packages of 0.5x0.5x0.5 mm^3 volume were fabricated in a 5x5 array as a process demonstration (process scalable to wafer level). The packages survived >72 h in 80ºC API brine, and separately high pressure condition of 200 MPa (29,000 psi).

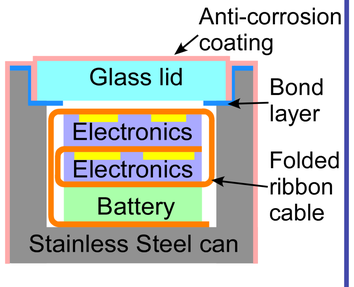
1 0.8-mm Packages: Design, Fabrication & Testing

Concept and Design

Parameter	Targets
Pressure	17 - 52 MPa (2,500-7,500 psi)
Temperature	75 - 125 ˚C
Salinity	API standard brine (8 wt% NaCl & 2 wt% $CaCl_2$)
Volume	<1 mm^3 exterior

- Package exterior dimensions: 0.8x0.8x0.8 mm^3; interior cavity dimensions: 0.4x0.4x0.45 mm^3
- High strength stainless steel (SS) 17-4 PH for metal can; glass lid for optical communication
- Folded flexible cable for integration of sensor & circuit chips
- Anti-corrosion coating

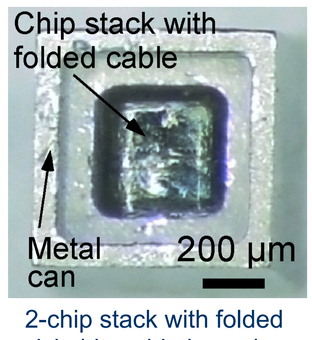




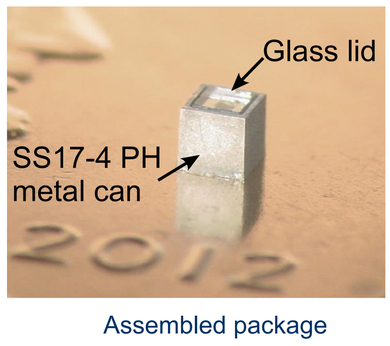
Ma, JMEMS 2015

Fabrication & Test Results

- Stainless steel cans fabricated by micro electro discharge machining (μEDM)
- Au-In eutectic bonding for hermetic package sealing
- Packages with anti-corrosion coatings survived >48 h in 80ºC API brine (8 wt% NaCl & 2 wt% $CaCl_2$), followed by 50 MPa (7250 psi) high pressure, and then 125ºC high temperature, without loss of hermeticity.

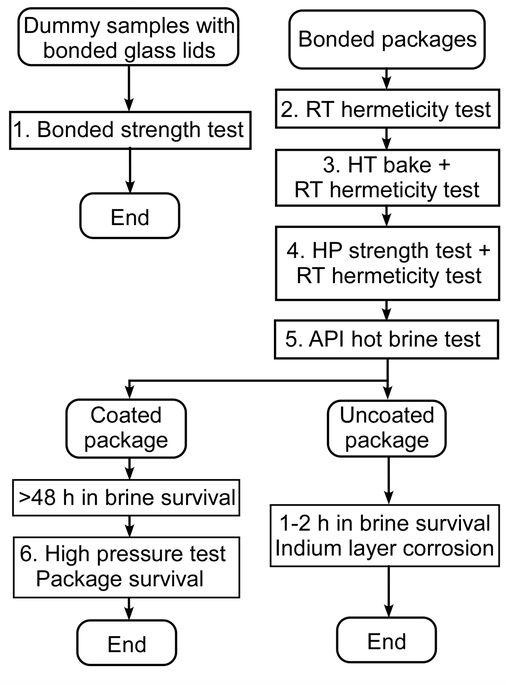


2-chip stack with folded polyimide cable in package



Assembled package

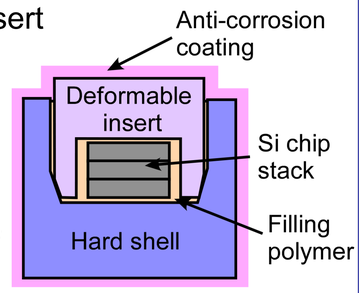
Package Test Flowchart



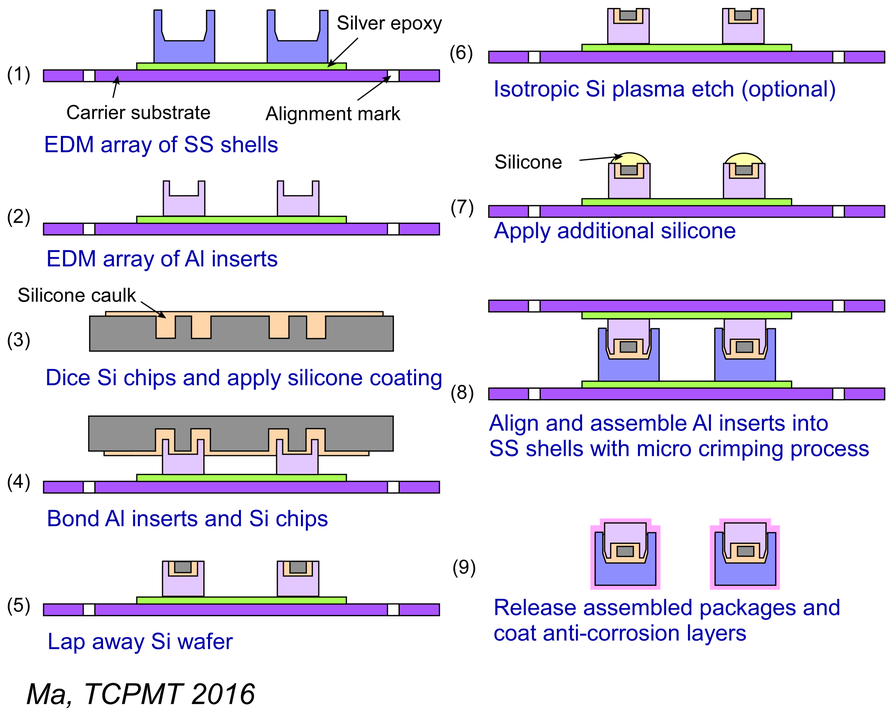
2 0.5-mm Packages: Room Temperature Batch Mode Packaging Process

Concept and Design

- Micro crimping packaging: Hard SS 316 shell + deformable Al insert
- Package exterior dimensions: 0.5x0.5x0.5 mm^3; interior cavity dimensions: 0.24x0.24x0.1 mm^3
- Anti-corrosion coating
- RF transparency for communication: For 2 MHz RF signal, skin depth of SS 316 ≈300 μm

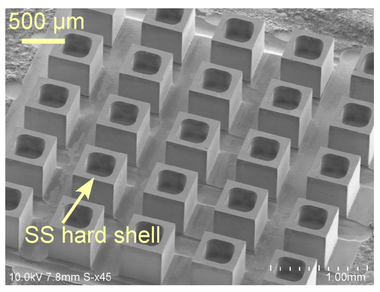


Process Flow

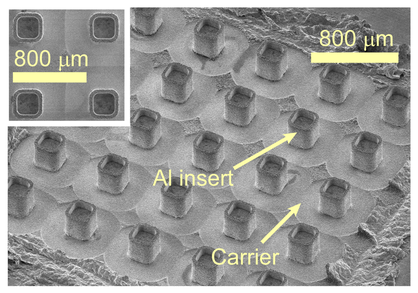


Ma, TCPMT 2016

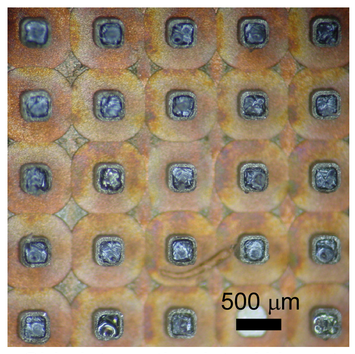
Fabrication Results

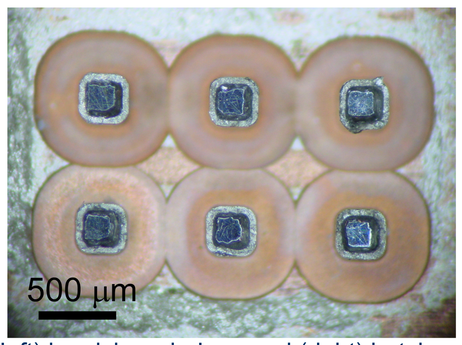


Array of SS hard shells
Outer: 500 x 500 x 500 $μm^3$
Inner: 340 x 340 x 300 $μm^3$

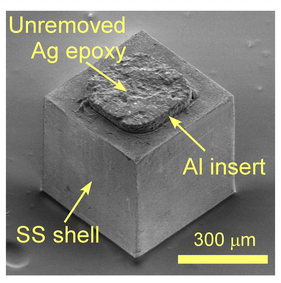


Array of Al deformable inserts
Outer: 330 x 330 x 320 $μm^3$
Inner: 240 x 240 x 100 $μm^3$

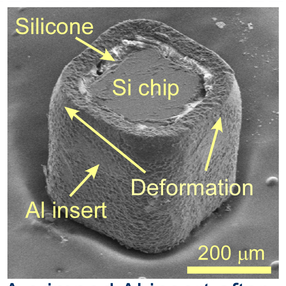




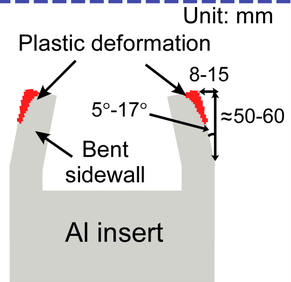
Chip integration into Al inserts: (left) by pick-and-place and (right) batch mode integration



A finished package



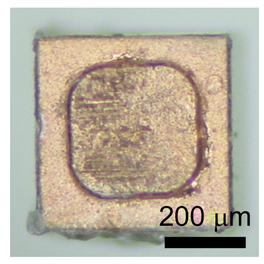
A crimped Al insert after separation from an assembled package



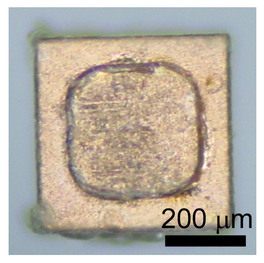
Typical micro crimping results

Test Results

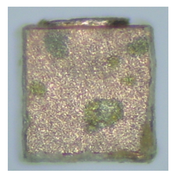
- Corrosion test
  - Test condition: 80ºC API brine
  - Package survived >72 h



Before test

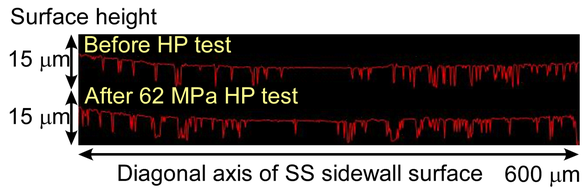


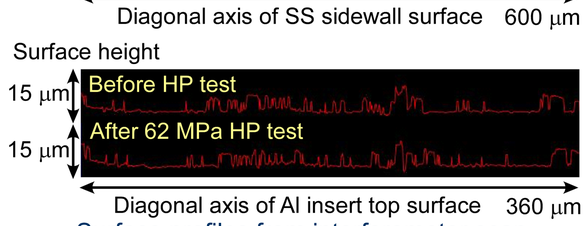
After 72 h in brine



Cu layer deposited under anti-corrosion coatings. Discoloration occurs when corroded (for comparison).

- High pressure test
  - Test condition: 62 & 200 MPa pressure
  - No package deformation
  - No crack in Si chip





Surface profiles from interferometer scan

Acknowledgement

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Patent Application

Packaged Microsystems, PCT Intl. Patent Application No. PCT/US2015/021100, submitted 2015; US Nationalization Patent Pending, Application No. 15/127,237, submitted Sep. 2016.

Publications

[1] Y. Ma, Y. Sui, T. Li, Y. Gianchandani, "A Sub-Millimeter Package for Microsystems in High-Pressure and High-Salinity Downhole Environment," *IEEE/ASME Journal of Microelectromechanical System*, vol. 24, no. 4, pp. 861-869, 2015.

[2] Y. Ma, T. Li, Y. Gianchandani, "A Low Temperature Batch Mode Packaging Process for Submillimeter Microsystems in Harsh Environment Applications", *IEEE Transactions on Components, Packaging and Manufacturing Technology,* vol. 6, no.3, pp. 366-372, 2016.

WIMS²

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